Theory Towards an all-optical WDM slotted-ring MAN with support for optical multicasting

Diptish Dey

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TOWARDS AN ALL-OPTICAL WDM SLOTTED-RING MAN WITH SUPPORT FOR OPTICAL MULTICASTING

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Dit proefschrift is goedgekeurd door:

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To my daughter, Deepshikha

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Diptish Dey
Enschede, The Netherlands
June 2003

Preface

Optical networking has proved to be one of the vital links in the Internet revolution that began in the last two decades of the twentieth century. The ability of optical networks to efficiently and cost-effectively deliver vast amounts of data is unquestionable. These networks have proved to be the cornerstone of high-speed data transmission. Yet there are attributes and concepts within the architecture of these networks that have proved to be the bottleneck in unleashing the total benefits of optical networking. One such attribute of present-day optical networks is electronic processing at intermediate nodes. Electronics is struggling to keep up with the high speed data transfer capacity of optical fibers and optical elements within the network. The optical network within the core has already developed by leaps and bounds over the last decade. The focus has currently shifted to the metropolitan area, where the bottleneck is concentrated.

The requirements for next-generations metropolitan area optical networks are varied. Some of them include support for data and voice services, enabling quality of service, supporting multicasting in the optical domain and partially or completely removing the electronic bottleneck. The end of the twentieth century saw a variety of proposals to reduce electronic processing at nodes within a metropolitan area network. However, most of these proposals fail to deliver a total end-to-end all-optical network. In this thesis, a novel network architecture has been proposed that removes the electronic bottleneck partially and enables support for all-optical multicasting in the nodes.

The network is based on interconnected dual counter-rotating fiber rings. Nodes residing on a ring have access (send and receive) to all wavelengths within both fibers in the ring. Time slots are used to transport data packets from a source node on a ring to a destination node on the same/another ring. If the destination node is on the same ring as the source itself, then the transfer of the data-packet is all-optical. However, if the destination node lies on a different ring in relation to the source, there is electronic buffering of the data packet when it crosses over from one ring to another. Slots emptied-out at a destination node can be re-used at the same node, enabling spatial reuse of slots. Spatial reuse of slots increases the overall throughput of a ring.

Enabling such an architecture leads to problems such as signal-to-noise ratio degradation, chromatic dispersion, crosstalk accumulation to mention a few. In the dissertation it has been shown using simulation techniques and laboratory experiments that signal-to-noise ratio degradation seriously impedes the scalability of a ring in terms of the number of optically transparent nodes it is able to potentially support. One of the requirements of the network architecture proposed here is that slots across all wavelengths must at all times be synchronized. Chromatic dispersion leads to slots losing their mutual alignment. A correction mechanism has been proposed and demonstrated in the laboratory. Reuse of slots at destination nodes lead to optical inband crosstalk. This crosstalk can be reduced by the usage of dilated switches or by postponing slot-reuse to a downstream node in relation to the destination node. However, the latter has implications on network utilization and throughput.

Based on laboratory demonstrations it can be concluded that the concept of using synchronized time-slots to transport data packets is practically feasible. It has been concluded from simulations and laboratory experiments that the main constraint in scaling the ring is due to signal-to-noise ratio degradation (resulting from the inherent all-optical nature of the ring).

Contents

List of Figures

List of Tables

CHAPTER 1

Introduction

This thesis addresses the architecture and design of slotted ring all-optical metropolitan area networks. The network may comprise of two or more interconnected rings. Access to the network is via nodes that store and forward data packets from and to the rings, implying opto-electronic conversion and back. However, these nodes are optically transparent to data packets that bypass them and remain on the ring. The nodes also support optical multicasting. Scalability of such a ring in terms of the number of nodes that it can potentially support has been addressed via simulation techniques and laboratory experimentation. A few concepts of the node functionality have also been experimentally demonstrated.

Section 1.1 presents a short summary on the history of optical networks and some of the key technologies that led to its successes. Optical networks in metropolitan areas are discussed in section 1.3 from their functional perspective and also from their requirements point-of-view. Finally, section 1.5 presents a brief overview of each of the chapters of the thesis.

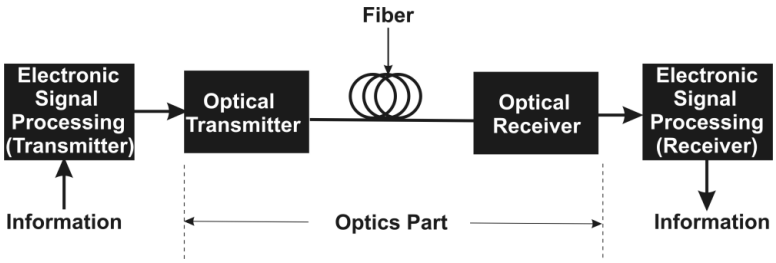

Figure 1.1: Block diagram of a single channel fiber optic link

1.1 Optical Networks

1.1.1 A brief history

Over the last century telecommunication networks have evolved through technological leaps and social changes. In the early 20th century the networks that just provided voice services via a local operator have metamorphosed into transmitting a colossal amount of voice, video and data traffic today. In 1966 Charles Kao predicted that the first major problem with fiber optic communications was the high attenuation of the fiber itself. Experimentally Kao managed to reach a low of 1000 dB/km. Kao laid out the clear major technical problems to be solved. It became clear that the key issue was manufacturing optical glass with very low loss. Robert Maurer, Donald Keck and Peter Schultz of the Corning Glass Corporation managed to bring down the attenuation to 20 dB/km in 1970. In due course of time with the invention of the chemical vapour phase deposition (CVPD) the attenuation has come down steadily. Today fibers with a loss of 0.2 dB/km around 1.5 μm are very common. Two other major components, the light source and the photo-diode matured hand-in-hand and by the time the optical fiber had levels of attenuation of 3 dB/km or less, light emitting diodes and lasers and photodiodes had become commercial. The basic diagram of a fiber optic communication system is shown in figure 1.1. In 1975 the first field trial of a fiber optic point-to-point communication system was conducted at Bell-Laboratories. In 1983 the first inter-city fiber link was established between New York and Washington D.C. In 1988 the first transatlantic fiber link was laid. Since then considerable research and development activity has been focused towards new technologies, which have provided the foundations of building optical networks. By the end of 1999, the total amount of fiber laid was equal to 75 million miles.

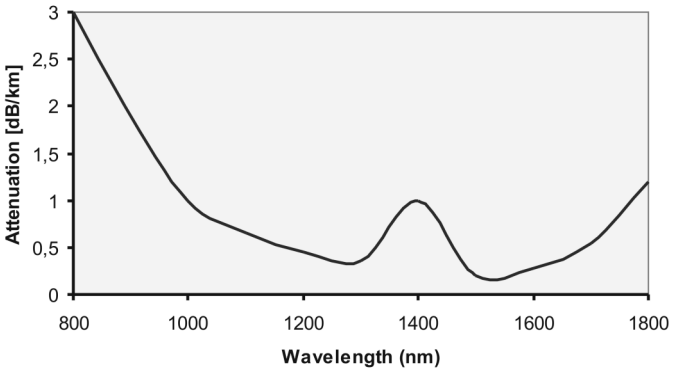

Figure 1.2: Typical attenuation profile of standard single mode optical fiber

1.1.2 Enabling Technologies

Two key technologies that have contributed to the success of optical networks are wavelength division multiplexing (WDM) ([Agr'97]) and the erbium-doped fiber amplifier (EDFA) (refer [BOS'99]). WDM enables the transmission of non-overlapping wavelength (or frequency) bands across the optical transmission spectra of optical fiber (see figure 1.2). Each of these multiple co-existing channels can be operated at a bit rate of upto 40 Gbps in commercial electrically time-domain multiplexed systems over a few hundreds of kilometers. Currently, available systems support from 32 to 64 channels and vendors are already offering up to 160 channel systems. This enables a single fiber to carry more than a terabit/s of information. The term dense wave division multiplexing (DWDM) is often used to describe systems supporting a large number of channels with the channels very tightly spaced. The inter-channel gap is typically 1.6 nm or 0.8 nm or less, corresponding to 200 GHz, 100 GHz or less in the 1.5 μm wavelength window. In contrast, the use of two or four channels, very widely spaced, on a fiber is sometimes referred to as "coarse" WDM (CWDM).

WDM technology provides obvious benefits by increasing the capacity of existing optical fiber and thereby reducing or avoiding the need to install additional fiber. However, the attenuation of fiber necessitates the use of repeaters at regular intervals to compensate for power losses. Converting an optical signal and reamplification, reshaping and retiming (3R) in the electronics domain is one solution. This implies the need for electrical regeneration of optical signals in long-haul networks and across all channels. The introduction of EDFAs

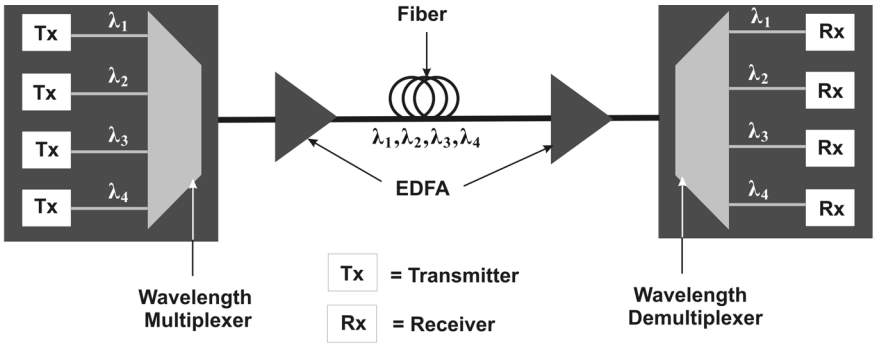

Figure 1.3: A typical WDM system

in conjunction with WDM systems has significantly reduced the total cost of high-capacity, long-haul networks. A single EDFA is able to reamplify all of the channels on a WDM fiber without the need to de-multiplex and process them individually, with a cost approaching that of a single regenerator. The EDFA merely amplifies the signals, and does not reshape or retime them as a regenerator does. One EDFA on a 40-channel WDM system can potentially replace 40 separate regenerators.

In addition to dramatically reducing the cost of regenerators, optical amplifiers and WDM systems greatly simplify the process of turning up additional channels. All that is required is to install additional transponders in the WDM systems at either end of the WDM links. The existing optical amplifiers simply amplify the new channel along with the others, without the need for additional regenerators. Figure 1.3 shows the block diagram of a typical WDM system with EDFAs to compensate for power loss. These cost savings generally more than offset the cost of WDM terminals themselves, and consequently virtually all long-haul network operators are deploying WDM technology.

In the late 1980s the Internet was incubating. By the 1990s IP (Internet Protocol) data traffic over the Internet was growing exponentially. The complex function of transporting IP packets from a source to a destination reliably and efficiently implied defining protocols to handle the tasks at different stages in the transfer of the packets. What soon emerged was the Internet protocol stack comprising of five independent layers handling the various functions involved in transfer of data packets. In the following section we discuss these layers briefly.

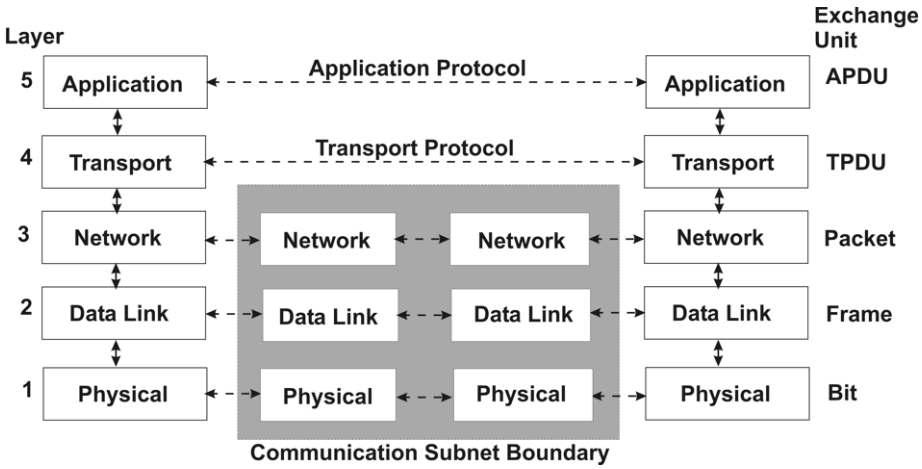

Figure 1.4: Network Architecture based on the IP Stack

1.2 The Communication Subnet

1.2.1 The Internet Protocol stack

Modern computer networks are designed in a highly structured way. To reduce their design complexity, most networks are organized as a series of layers, each one built upon its predecessor. The Internet consists of five layers. Protocol layering has structural and conceptual advantages. However, duplication of functions by higher layers is a serious concern. For further details refer to [WCW+'92]. The layers are:

- Application : Supports network applications; protocols including HTTP (Hyper Text Transfer Protocol), FTP (File Transfer Protocol) and SMTP (Simple Mail Transfer Protocol).

- Transport : Provides end to end communication control; protocols include TCP (Transmission Control Protocol) and UDP (User Datagram Protocol).

- Network : Routes IP packets within the network from one host to the other; protocol includes the celebrated IP protocol.

- Data Link : Moves frames from one network element to the other; protocols include Ethernet, ATM (Asynchronous Transfer Mode), SONET/SDH

(Synchronous Optical Network/Synchronous Digital Hierarchy) and others.

- Physical : The transmission media for actual transfer of bits between network elements; examples fiber, copper, air (for wireless), transmitters, receivers and others.

Figure 1.4 shows these layers. For the sake of this dissertation, our discussion is focused on the bottom three layers. For further reading on this topic please refer to [KR'01]. The physical layer is concerned with transmitting bits over a communication channel. The design issues have to do with making sure that when one side sends a 1 bit, it is received by the other side as a 1 bit, not as a 0 bit. The main task of the data link layer is to take a raw transmission facility and transform it into a line that appears free of transmission errors in the network layer. It accomplishes this task by having the sender break the input data up into data frames (typically a few hundred bytes), transmit the frames sequentially, and process the acknowledgment frames sent back by the receiver. Since the physical layer merely accepts and transmits a stream of bits without any regard to meaning of structure, it is up to the data link layer to create and recognize frame boundaries. This can be accomplished by attaching special bit patterns to the beginning and end of the frame. If there is a chance that these bit patterns might occur in the data, special care must be taken to avoid confusion. The data link layer should provide error control between adjacent nodes. In the network layer a key design issue is determining how packets are routed from source to destination. Routes could be based on static tables that are "wired into" the network and rarely changed. They could also be determined at the start of each conversation, for example a terminal session. Finally, they could be highly dynamic, being determined anew for each packet, to reflect the current network load.

For an understanding of this dissertation understanding of SONET/SDH, among other concepts, is particularly essential. The following section is devoted to this data link layer protocol.

1.2.2 SONET/SDH

In the early days of fiber optic networks, each telephone operator had its own proprietary optical time-division multiplexed (TDM) system, yielding a number of Plesiochronous Digital Hierarchy (PDH) standards. But with the break-

up of AT&T in 1984, operators faced the problem of connecting across different optical TDM systems. In 1985 Bellcore started working on a standard to help connect different network operators at the data link layer. It was named SONET (Synchronous Optical NETwork). Later a compatible version, referred to as SDH (Synchronous Digital Hierarchy) was published by ITU-T (International Telecommunication Union - Telecommunication Standardization Sector) in Recommendation G.707. The SDH recommendations differ from SONET only in minor ways. Virtually every public network in the world today runs SONET/SDH.

Behind the effort of creating SONET/SDH lay four major goals. First, SONET/SDH made it possible for different carriers to interwork. This meant defining a common signaling standard with respect to timing and framing structure, to mention only a few. Second, it provided the means to unify the U.S., European and Japanese digital systems. Third, there was a need to multiplex multiple digital channels at different speeds in a hierarchical manner. Fourth the complexity of the network had to make way for better operations, administration and maintenance (OAM). SONET/SDH also considerably simplified networking functions such as add-drop crossconnects. Network management also became easier with the adoption of SONET/SDH. The SONET/SDH standards being able to support all the above requirements and many more, made it a technology deeply rooted in the heart of the telecommunications industry. For more information on SONET/SDH refer [LK'02]

With the maturity of the optical network in the long-haul networks (where speed of data transfer and manageability are the buzz words), the need arose to look into potential bottlenecks that appear in the network during data transfer from one host to another. Today this bottleneck lies in the metropolitan area network (MAN). The following section looks at the use of optical networks in MANs.

1.3 The Metro Optical Space

Metropolitan Optical Networks (MONs) are characterized as networks that move traffic within the metropolitan area, and into and out of the core network and customer access networks. These networks have increasingly gained importance from the operator's point of view for they bridge the gap between the core and the access networks. This has far-reaching implications because

of the diverse types of access networks that a MON typically has to support. Diverse types of customers on the MON imply diverse requirements and the technology needs to support these requirements. [MDD+'00] and [MDD+'02] provide a similar study on the requirements imposed by human behaviour, for instance, on the design of LANs (Local Area Networks). An efficient MON operator must be able to upgrade capacity demands made by its clients on the MON cost-effectively and with minimum latency and effort. Today Metropolitan Optical Networking is a lucrative market opportunity. The advantages of successful deployment of WDM accompanied by packet switching in the MON are incontrovertible. To assist in this evolution, it is clear that a new and innovative transport architecture is required.

1.3.1 Functional Perspective

The metro network is expected to support a number of protocols and services. The different attributes of these services pose a challenge for the transport equipment and architecture. Common categories of services include SONET/SDH, ATM, Ethernet, and storage. A few functional architectures for the metro optical space will be considered here.

In the DWDM Overlay approach (shown in Figure 1.5), each protocol is independently mapped into a wavelength and placed upon the DWDM layers. This results in a very transparent and simple approach. However, an under-utilized protocol implies wasting expensive DWDM resources. There is no mutual interworking or multiplexing layer, which makes it even more difficult to provision and manage.

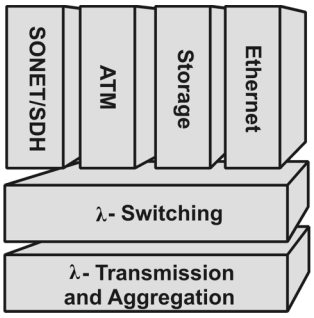

Figure 1.5: DWDM-Overlay

Usage of existing SONET/SDH rings led to the situation shown in Figure

1.6. This implies packing all protocols into TDM and then putting them into SONET/SDH frames. This comes with having to deal with reduced flexibility and increased complexity. For service providers to do any kind of provisioning is very difficult. Ethernet often leads to large frames, which have to be squeezed into time-slots. The advantage for operators is that the OAM functions can be handled by the SONET/SDH layer in a standardized way.

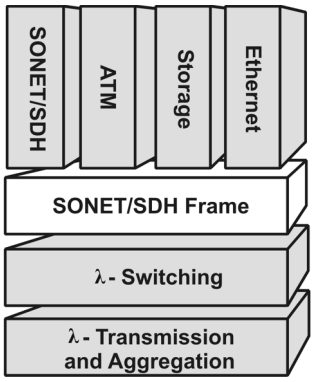

Figure 1.6: SONET/SDH Overlay

Other approaches include replacing the SONET/SDH Frame layer in Figure 1.6 with an Ethernet MAC (Medium Access Control) or by using MPLS (Multi Protocol Label Switching) labels (see chapter 2, section 2.4.2). Each of them comes with its own advantages and disadvantages. The advantage of using an Ethernet MAC is that it is the natural way to transport Ethernet/IP traffic. Storage protocols are not supported at all. Using MPLS labels greatly enhances the flexibility of packing services into wavelengths while transporting services in their native formats.

1.3.2 Requirements for Next-generation MANs

Next-generation MANs must meet the following requirements:

- *Scalability*: Ability to scale to high bandwidths and large number of network nodes. For today's networks this implies tens of Gigabits per second (Gbps) of bandwidth per link and large numbers of nodes implying many more than the 16-node limit of traditional Synchronous Optical Networking (SONET) or Synchronous Digital Hierarchy (SDH) solutions.

- *Low Cost*: Low installation and operational costs as well as low cost per Gbps.

- *Support for next-generation differentiated services*: The network must be able to provide differing levels of service by defining and maintaining Service Level Agreements (SLAs). This in turn requires support for service creation and monitoring/billing/control capabilities in order to achieve QoS (Quality of Service) control. The network must also support a range of physical interfaces.

- *Support for legacy voice services*: Traditional circuit-switched voice is still an important revenue bearing service, although it accounts for a decreasing percentage of total bandwidth.

- *Powerful, easy-to-use network management*: Network management must provide extensive control and monitoring facilities yet be easy to provision and operate. The network management system must also provide protection against misconfiguration, a cause of many network performance problems and outages. It also has to provide network restoration functionalities.

- *Robustness*: Redundant hardware, and fiber protection/restoration.

1.3.3 Considerations in building a MAN

We make a number of assertions about the right way to build a MAN:

- *Optimized for IP transport*: IP is increasingly becoming the most dominant type of traffic in today's networks and its presence is only expected to increase further in the next-generation MANs. Optimizing for IP transport enables flexibility in service creation and support as well as minimizes equipment and operating costs.

- *Packet-switched*: Packet-switched technologies provide efficiency and gain through statistical multiplexing and thus are cost-effective, flexible and scalable. They are also the most optimal way to transport IP traffic.

- *Backwards compatibility with legacy transport*: A successful MAN solution should not only be optimized for IP transport, but must also support legacy transport, most notably circuit-switched voice and video.

- *QoS*: In order to provide acceptable QoS guarantees it is necessary to integrate intelligent traffic planning with underlying resource management mechanisms like queuing engines, schedulers and ingress traffic policing.
- *Minimize circuit-switched layers*: Extra circuit-switched layers add unnecessary system complexity and cost, thereby, decreasing network efficiency, and making network provisioning more complex and time-consuming.
- *Provide Restoration Functionalities*: Fault detection and re-routing.

1.3.4 Standardization Efforts

Efforts have been made to drive some standardization within metro area networks. Quite recently, the ITU-T Recommendation G.694.2 set the standard for the wavelengths to be used in MANs to be used in CWDM systems. Unlike DWDM, in which wavelengths are spaced less than a nanometer apart, the new standard for CWDM specifies 20-nm spacing. The implications of this wider spacing are twofold. Keeping such a high channel spacing implies that the lasers and the filters that form an integral part of a WDM system have greater wavelength tolerances, for example, the temperature drift of lasers can be a bit relaxed. On the other hand the components should become cheaper with such a relaxed channel spacing.

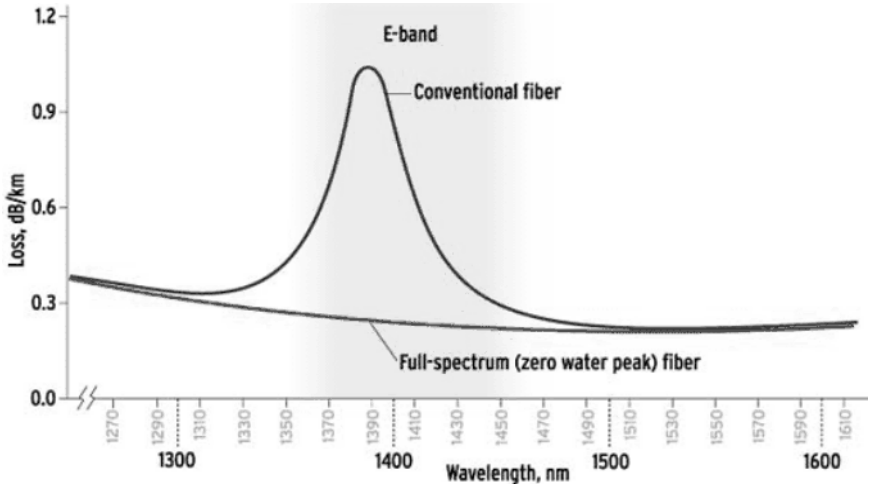

Figure 1.7: CWDM Wavelengths: The figure has been obtained from [Rie'02]

The CWDM grid explicitly defines only 18 wavelengths, from 1270 nm to

1610 nm (shown in figure 1.7), whereas dense systems squeeze hundreds of channels into a single fiber. But the technology is a good match for metropolitan-area networks, which do not need the huge capacity of long-haul DWDM systems. Using standard single-mode fiber with the standardized CWDM set of wavelengths could mean not using a few wavelengths because of the water-absorption peak. Fortunately full-spectrum fibers like AllWave and SMF-28e are in commercial use. With those fibers well established and the new ITU Recommendation ensuring stable technical specifications, the stage is set for rapid growth in metro-area networking.

1.4 The Research Project

This thesis and the research work associated has been accomplished within the scope of two broad projects. First is the FLAMINGO (Flexible Multi-wavelength Optical Local Access Network Supporting Multimedia Broadband Services) project supported by the Dutch Technology Foundation, STW. The second project is a partnership between KPN (Royal Dutch Telecom) and the University of Twente (UT).

The FLAMINGO project had three main work areas. These include device technology, physical layer techniques, and protocol and networking design. Within the latter it was required to study and develop system concepts for broadband (Gb/s) optical networks. The design and realization of a demonstrator is part of the FLAMINGO project. However, in order to limit the project costs, the basic feasibility of the approach would be demonstrated by implementing the key functionality of a network node complemented with functional simulations of an entire network. Simulation in software would be used to study the functional behavior and the performance of a complete network starting from measurements performed on the single node prototype.

KPN's interest and its support towards the completion of this work was crucial. As an experienced operator in the metro space KPN engineers provided knowledge, financial and material support to complete the work in a more practical way. Understanding the key issues facing them was important in realizing the concept of the metropolitan all-optical network.

1.5 Outline of the Thesis

This thesis is arranged as follows.

Chapter 1, this chapter, gave a brief introduction to the thesis. It started with a brief history of optical networking and a few key technologies that paved the way for its success, including its present form. Subsequently requirements and considerations of building an optical network in the metropolitan area were discussed. Finally we gave an overview of the projects within which this research work has been accomplished.

Chapter 2 provides an overview of network architectures for building IP over WDM networks. It discusses relevant technologies and proposes a novel network architecture enabling, among other things, an all-optical ring with packet-switching, IP over WDM, and multicasting in the optical domain.

Chapter 3 focuses on the architecture of the node. The nodes reside on the all-optical ring. They enable data packets to be added to or dropped from the ring or let packets arriving from upstream nodes reach downstream ones. Apart from this functionality the node also compensates for dispersion effects and enables construction of optical multicast trees. The chapter also discusses the preferred components to be used to build the node.

Chapter 4 resorts to simulation techniques to simulate the performance of the network and the node. For this purpose commercial simulation software, *VPITransmissionMaker* and *VPIComponentMaker*, from Virtual Photonics Incorporated (VPI) has been used. The electronic functionality at the node has also been simulated in order to be finally implemented on an Altera FPGA (Field Programmable Gate Array). Towards the end of the chapter some analysis is provided to put the simulation results in a practical context.

Chapter 5 presents some laboratory results verifying essential concepts of the network architecture in the form of a demonstrator. Further experiments were performed and their results presented to verify certain optical performance parameters such as crosstalk and signal-to-noise ratio (SNR) degradation.

Finally in chapter 6 the conclusions of this thesis are presented. The chapter also provides some directions for further research.

CHAPTER 2

Architecture for Packet-switched Networks

2.1 Introduction

WDM provides means for efficient utilization of the multi-THz bandwidth of optical fiber. Although as a transport mechanism in the core network its suitability is incontrovertible, its applicability to situations when bandwidth management is required is limited. WDM is essentially a circuit-switched technology. Nevertheless, when combined with other optical multiplexing techniques such as Code Division Multiplexing (CDM) [ZPS'00] and Sub-carrier Multiplexing (SCM) [JK'92], WDM can play important roles in enabling optical packet-switched network architectures. Such architectures enable flexible bandwidth allocation among the nodes leading to efficient multiple access schemes.

In the next section we first present an overview of physical layer network topologies. Subsequently we motivate our preference for the ring topology. In section 2.3 we discuss the limitations of existing SONET/SDH rings in transporting data packets within the metro space. Section 2.4 presents an overview of IP-over-WDM architectures. Section 2.5 presents two state-of-the-art technologies in the MAN. In section 2.6 we motivate our preference for packet-based

network architectures. We present the concept of the slotted-ring network, its principles of operation, and its ability to support optical multicasting in section 2.7. Here we also discuss interconnected slotted-rings. Finally, in section 2.8 we present a few concluding remarks.

2.2 Network Topologies

The topology of a network defines how the nodes of the network communicate with one another over the physical media. There are five major topologies in use today: Bus, Star, Ring, Tree, and Mesh. Each is used for specific network types, although some network types can use more than one topology. For example, Ethernet [I802.3] networks can be laid out in a Bus, Star, or Tree topology, or any combination of the three. Each topology has its own strengths and weaknesses.

Bus

With the Bus topology, all workstations are connected directly to the main backbone that carries the data. Traffic generated by any computer will travel across the backbone and be received by all workstations. This works well in a small network of 2-5 computers, but as the number of computers increases so will the network traffic and this can greatly decrease the performance and available bandwidth of the network. 10Base-2 ("ThinNet") and 10Base-5 ("ThickNet") both were popular Ethernet cabling options years ago. However the biggest drawback is that the entire network shuts down if there is a break in the main cable and it is difficult to identify the problem in such an event.

Star

The Star or Hub topology is one of the most common network topologies found in most offices and home networks. It has become very popular in contrast to the bus type, because of the cost and the ease of troubleshooting. A star topology consists of a point-to-point connection to a central connection, generally a hub or a switch. A hub may have two or more connectors, which allow two or more network nodes to be connected to the network. Devices typically connect to the hub with Unshielded Twisted Pair (UTP) Ethernet. The advantage of the star topology is that if one computer on the star topology fails, then only the

failed computer is unable to send or receive data. The remainder of the network functions normally. The disadvantage of using this topology is that because each computer is connected to a central hub or switch, if this device fails, the entire network fails.

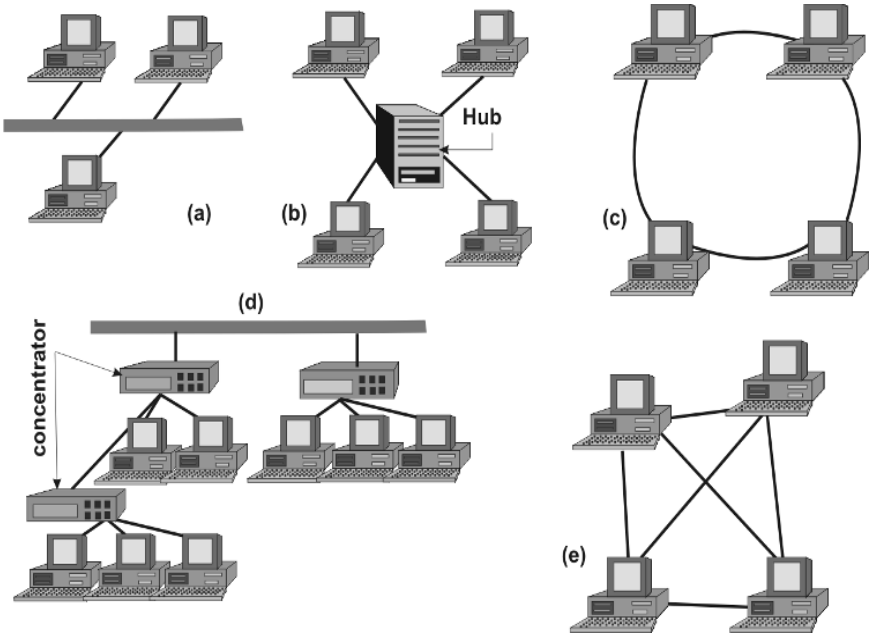

Figure 2.1: Network Topologies: (a) bus; (b) star; (c) ring; (d) tree; (e) mesh

Ring

In a ring network, every device has exactly two neighbors for communication purposes. All messages travel through a ring in the same direction (effectively either "clockwise" or "counterclockwise"). The ring topology has many of the same problems as the bus topology, in that it can be difficult to troubleshoot and a single break can disable the whole network. A double counter-rotating ring can however be used for protection. To implement a ring network, one typically uses FDDI (Fiber Distributed Data Interface) [Mil'95], SONET/SDH [LK'02], or Token Ring [I802.5] technology. Rings are found in some office buildings or school campuses and in MANs.

Tree

A tree topology combines characteristics of linear bus and star topologies. It consists of groups of star-configured workstations connected to a linear bus backbone cable. Tree topologies allow for the expansion of an existing network. Its main drawback is that if the backbone line breaks, the entire segment goes down. A Passive Optical Network (PON) is the best example of a network with a tree topology. Trees can also be multihop if splitting nodes process the signal.

Mesh

Mesh topologies involve the concept of routes. Unlike each of the previous topologies, messages sent on a mesh network can take any of several possible paths from source to destination. This provides a great improvement in performance and reliability, however the complexity and difficulty of implementation increases geometrically as the number of nodes on the network increases. For example, a three or four node mesh network is relatively easy to realize, whereas it is impractical to set up a full mesh network of 100 nodes – the number of interconnections would be so high and expensive that it is not practical. Mesh networks are not used much in LANs but are used in Wide Area Networks (WANs) where reliability is important and the number of sites being connected together is fairly small. A mesh may also be logically configured to be a concatenation of rings.

Figure 2.1 shows the above topologies. The advantage of a double ring topology over others include fast protection and restoration. Also rings provide a natural multicast mechanism. Multicasting is considered in detail in 2.7.3. It is worthwhile to mention that fiber in MANs is mostly as rings. This is due to the existing SONET/SDH infrastructure. Future network architectures in the MAN space should take advantage of this fact. The network architecture proposed in section 2.7, which is the central idea of this dissertation exploits these advantages of ring-based topologies and existing ring infrastructure in MANs.

2.3 Limitations of SONET/SDH in the Metro Rings

Most metro fiber is in the form of rings. Ring topology is a natural match for SONET/SDH that exists in an overwhelming majority of today's metro networks. Some of SONET/SDH's advantages are:

- Fail-safe Architecture: SONET/SDH Service has to provide 99.99% error-free seconds, circuit reliability, and availability (up time). Its service has very good survivability. If a circuit on a dedicated ring goes down, it will automatically be protection switched within 50 milliseconds, so that customers will experience little or no service disruption; and,

- Manageability: SONET/SDH has highly developed diagnostics and control, making complete end-to-end network management and control possible.

SONET/SDH has withstood the tests of a time when voice was predominant in networks. Using TDM-based infrastructure fixed bit rate voice circuits were easily established, managed and transported between points in the network. Its 125 μs framing has been designed to be compatible with 64 kbps voice telephony. But with the advent of the Internet, data-traffic across these networks went up by leaps and bounds. SONET/SDH was proving to be a bottleneck. Its disadvantages include:

- Fixed Circuits: SONET/SDH provisions point-to-point circuits between nodes. These circuits are allocated a fixed capacity and are often under-utilized. For data traffic the problem is aggravated by its burstiness;

- Multicast Traffic: In SONET/SDH multicasting is possible if each source allocates a separate circuit for each destination. The multiple copies leads to waste of bandwidth;

- Large Provisioning Times: The complex hierarchy of grooming and cross-connect devices in the SONET/SDH infrastructure is expensive to deploy, maintain and scale. In addition it is time-consuming, cumbersome and expensive to provision and often requires long lead times. For example, an enterprise customer on a WAN who has a T1[1] (1.544 megabits per

[1]The term "T1" is also used colloquially to refer to the DS1 signal and "T3" to refer to

second) circuit today and outgrows it has two options: upgrade to T3 (45 megabits per second) or install another T1 circuit. The time required and the cost implied for either operation is quite big.

Thus the need for a more efficient architecture arises. Among other things, the new architecture must be easily scalable, must be optimized for IP transport and should be packet-switched. Placing IP packets directly over WDM is one of the solutions for efficiently handling IP traffic [Liu'02]. However, IP over WDM solutions often suffer from technological limitations and it will be sometime for them to be fully effective and deployable in the MAN [GDW'00]. In the following section we discuss a few IP over WDM architectures.

2.4 IP over WDM architectures

Present day WDM technologies exists in two broad forms: circuit-switched WDM and packet-switched WDM. In circuit-switched WDM there exists a light-path topology in which each lightpath behaves as an established circuit. The topology reconfigures itself based on traffic parameters and network planning. In packet-switched WDM optical headers and/or labels travels along with the data and are processed at switching points within the network.

Circuit-switched WDM finds its use mostly in backbone transport networks. This is because traffic in the backbone is less bursty. However, in LANs, MANs and access networks, traffic is very bursty and needs to be switched frequently. Here handling traffic efficiently and with minimum latency is the key. Flexible network architectures are a must in these networks. Packet-switched WDM networks aim at comprehensive and scalable network functions. Packet-switched WDM can be divided into 3 types: Optical Burst Switching (OBS) [QY'99], Optical Label Switching (OLS) [IETF01] and Optical Packet Switching (OPS) [RMGB'97], which we discuss next.

2.4.1 Optical Burst Switching

OBS is a natural way to support real-time multimedia traffic in the Internet which is often self-similar or bursty and requires low latency. It is especially

the DS3 signal. Plesiochronous Digital Hierarchy (PDH) developed 40 years ago by Bell Labs to carry digitized voice over twisted wire more efficiently. A PDH evolved into the North American Digital Hierarchy, which is known more commonly by its signal names DS0 through DS3.

economic and efficient for providing high-end users or applications with sessions having a high bit-rate, low latency and short duration upon their requests.

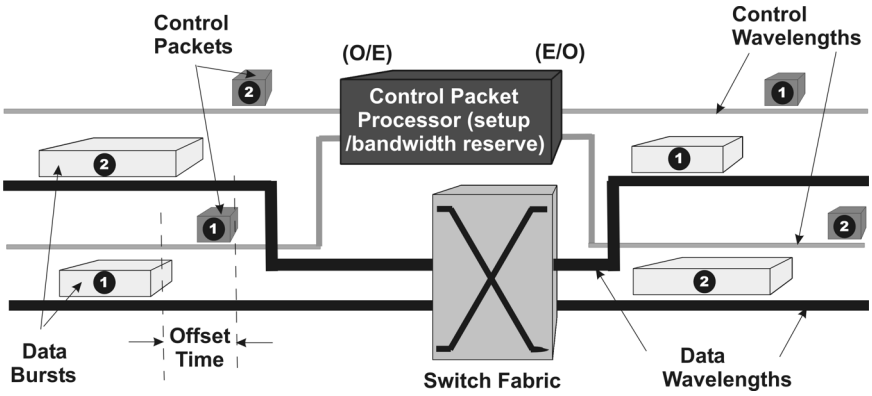

Figure 2.2: Optical Burst Switching

OBS uses one-way reservation so that a burst of user data (e.g. IP packets) can be sent without having a dedicated wavelength path in hand. Instead, a control (set-up) packet is sent first to reserve the wavelength channel, which is followed by the burst after an offset time. Intermediate nodes/switching points on receiving the control packet start calculating the next hop and reconfigure its underlying switching fabric before the burst of data packet arrives. This means that the delay between the control packet and its corresponding data packet (burst) has to increase with the number of hops. The basic operation of OBS is depicted in figure 2.2. Thus, unlike circuit-switching OBS not only avoids the long end-to-end setup delay, but also increases the utilization of the ultra-high speed optical channels for variable-bit-rate services. By combining the best of the coarse-grained optical circuit switching (e.g. via wavelength routing) and the fine-grained optical packet/cell switching while avoiding their shortcomings, OBS can potentially realize the vision of building a flexible, efficient and bandwidth-abundant fiber-optic network infrastructure capable of providing ubiquitous services to IP and other existing (e.g. ATM) and future protocols.

Current and near future research is needed to address several challenging issues including the designs and implementations of high-speed optical burst switching protocols and cost-effective burst-buffering mechanisms to achieve a high throughput with a low burst-dropping probability.

2.4.2 Optical Label Switching

Label switching is similar to burst switching except that it uses the MPLS approach, i.e., using local labels and forwarding traffic over label switched paths. MPLS uses a label switching forwarding method to direct packets through a network. In label switching, a packet is assigned a label and passes along a predetermined path of routers. Forwarding decisions are based on the contents of the label, rather than information in the packet's IP header.

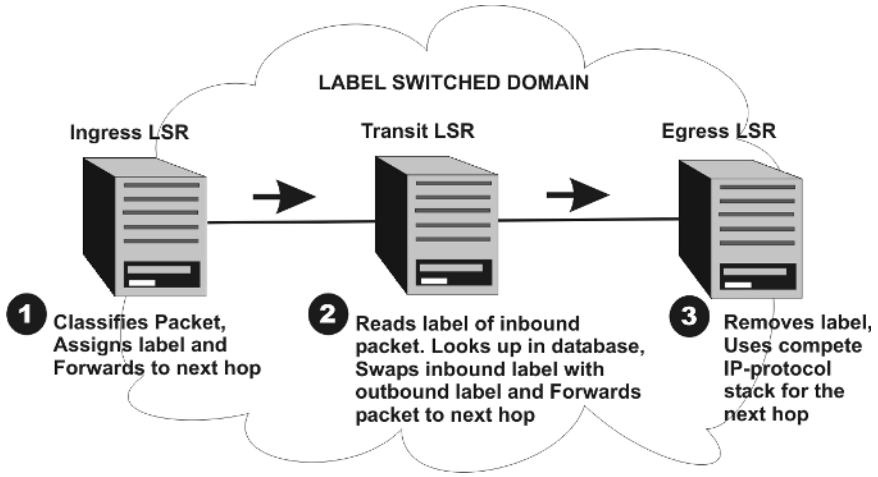

Figure 2.3: Label Switched Domain

An MPLS domain consists of a group of MPLS-enabled routers, called LSRs (Label Switching Routers). In an MPLS domain, packets are forwarded from one MPLS-enabled router to another along a predetermined one-way path, called an LSP (Label Switched Path). To provide two-way traffic, LSPs are configured in each direction. The path is set up in advance and packets or bursts of packets are routed along it using its labels.

The LSRs at the headend and tailend of an LSP are known as LERs (Label Edge Routers). The LER at the headend, where packets enter the LSP, is known as the ingress LER. The LER at the tailend, where packets exit the LSP, is known as the egress LER. In between the ingress and egress LERs there may be one or more transit LSRs. Figure 2.3 depicts an MPLS domain with a single LSP consisting of three LSRs: an ingress LER, a transit LSR, and an egress LER.

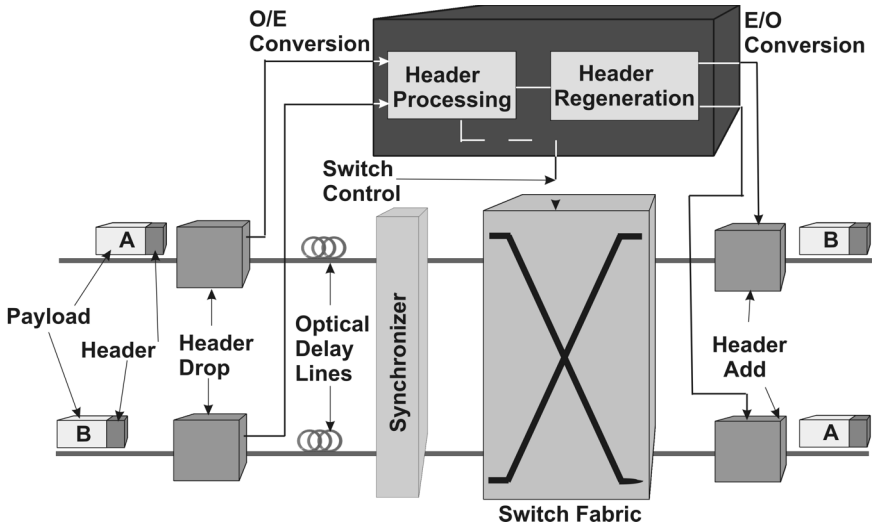

Figure 2.4: Optical Packet Switching

2.4.3 Optical Packet Switching

In OPS the packet control header is sent along with the data-packet. Upon arrival at an intermediate switching point in a network, the header is read and subsequently switching decision computations and changes to the underlying switch fabric are made. During this time the data packet is delayed in an optical delay loop. Figure 2.4 shows the operation of a OPS WDM system.

Within OPS there are two forwarding paradigms. In datagram forwarding, the packet header is read at each intermediate node. Here there is no offset time as the data and the header are sent out together. This is typical of IP. On the other hand virtual circuit forwarding involves setting up of virtual circuits before packets are sent over them. Each virtual circuit carries an identification number. Intermediate nodes have switching tables mapping incoming virtual circuits to an output port. Thus routing is separated from forwarding.

2.4.4 Networking Architectures

With IP data-traffic dominating networks, it is of utmost importance to have network architectures that transport IP traffic efficiently over WDM networks. Here we discuss three relevant architectures.

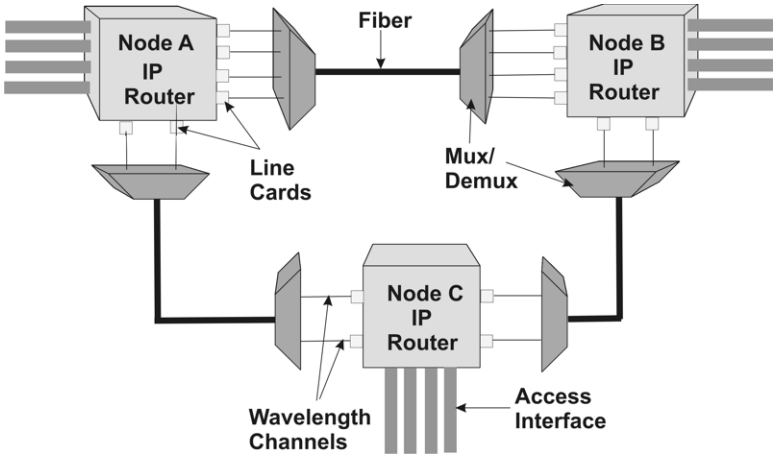

Figure 2.5: IP over Point to Point WDM

IP over Point-to-Point WDM

Within this architecture IP traffic runs over point-to-point links, running WDM. WDM devices such as OADMs (Optical Add Drop Multiplexers) do not form a network themselves. Their job instead is to link IP routers at the physical layer. Such systems are usually high capacity long-haul networks. The architecture requires IP routers to be directly connected to each other via multi-wavelength fiber links. This is shown in figure 2.5. The network topology is fixed and the network configurations are all static. IP packets are encapsulated in SONET/SDH frames using Packet-over-SONET schemes [And'02]. There is very little interaction between the IP and WDM layers. Such networks have been commercially deployed for over a decade now.

IP over Circuit-switched WDM

In this architecture IP router interfaces are connected to the client interfaces of the WDM network. Figure 2.6 shows the architecture. The OADMs and the OXCs (Optical Cross Connects) are interconnected to each other and form a WDM network, which has a physical topology and a lightpath topology. Network elements connected to each other form the physical topology whereas wavelength channel connections form the lightpath topology. Circuit-switched WDM is reconfigurable and allows channel set-up and tear-down in a controlled fashion. IP routing and wavelength switching never work in the same layer. Lightpaths in the WDM network are made to conform to the higher IP topology. Thus

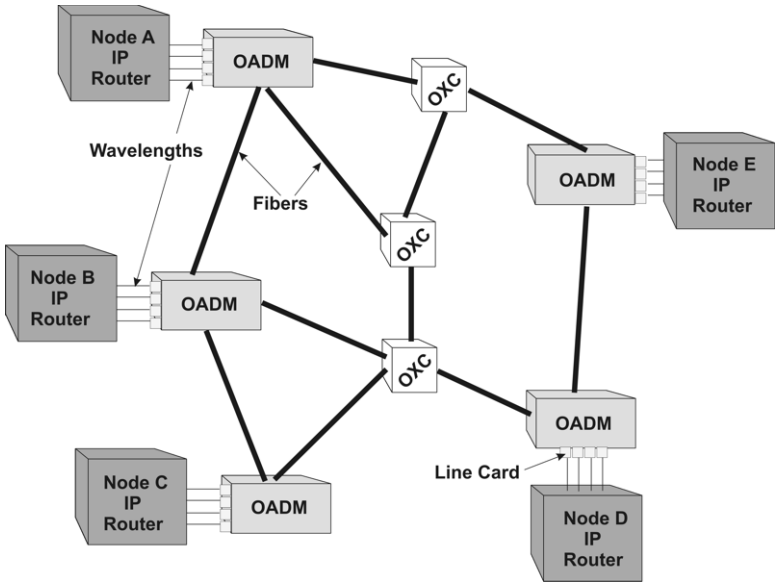

Figure 2.6: IP over Circuit-switched WDM

reconfiguring of OXCs enables a given router interface to be connected to any other router interface at any other router.

IP over Packet-switched WDM

In an IP-over-Packet-switched WDM architecture the network has the ability to switch on a per-packet basis. In sections 2.4.1, 2.4.2 and 2.4.3 various approaches such as OBS, OLS and OPS have been proposed. Figure 2.7 shows an overview of the architecture. In the figure OBS and OLS are combined and corresponding routers are indicated as OLSR (Optical Label Switched Router). OLSR is usually deployed in a cluster. Within the cluster, only the edge routers need to implement the complete IP protocol stack. The edge also buffers packets coming into the cluster so that a LSP is set up in the case of dynamic LSP setup.

The three architectures mentioned above have their own different control and management software. The IP over Point-to-Point WDM architecture is gradually replaced by the IP over Circuit-switched WDM architecture. The latter can provide higher network resource utilization, lower operational costs and higher functionality if installed with good network control software and traffic engineering.

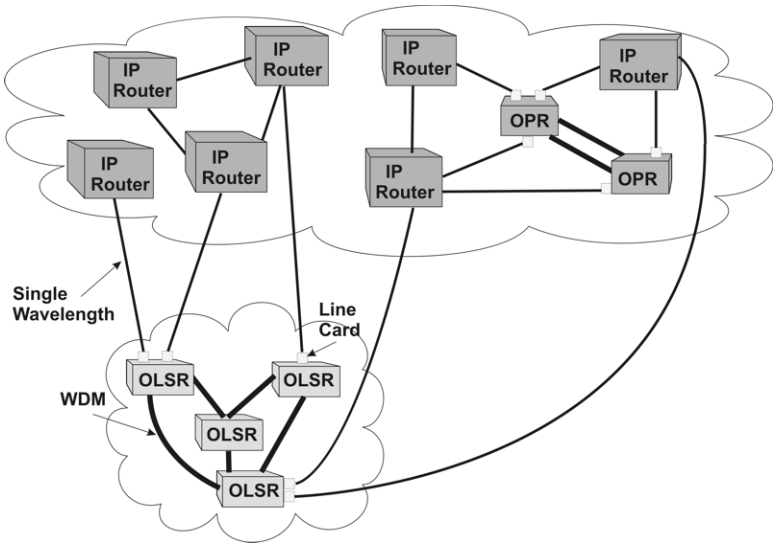

Figure 2.7: IP over Packet-switched WDM

2.5 Current Technologies

2.5.1 Resilient Packet Rings

Resilient Packet Rings (RPR) is an emerging network architecture and technology designed to meet the requirements of a packet-based metropolitan area network. Initial RPR products based on IETF (Internet Engineering Task Force) RFC (Request for Comments) 2892 – spatial reuse protocol (SRP) – have been deployed in networks worldwide. The IEEE 802.17 working group is currently defining an industry standard [I802.17] for an RPR MAC.

RPR – Overview of the Physical Layer

RPR technology uses dual counter-rotating fiber ring topology. Both the rings are used to transport working traffic between nodes. By making use of both fibers, instead of keeping one fiber spare for protection purposes, RPR exploits the total available bandwidth of both rings. Control messages, for example, bandwidth allocation, protection and topology discovery flow in the opposite direction of the traffic that they correspond to. The basic functioning of RPR is shown in figure 2.8. By using bandwidth-control messages, a RPR node dynamically negotiates for bandwidth with other nodes on the ring.

The principal advantages of such a topology include multicast-capability

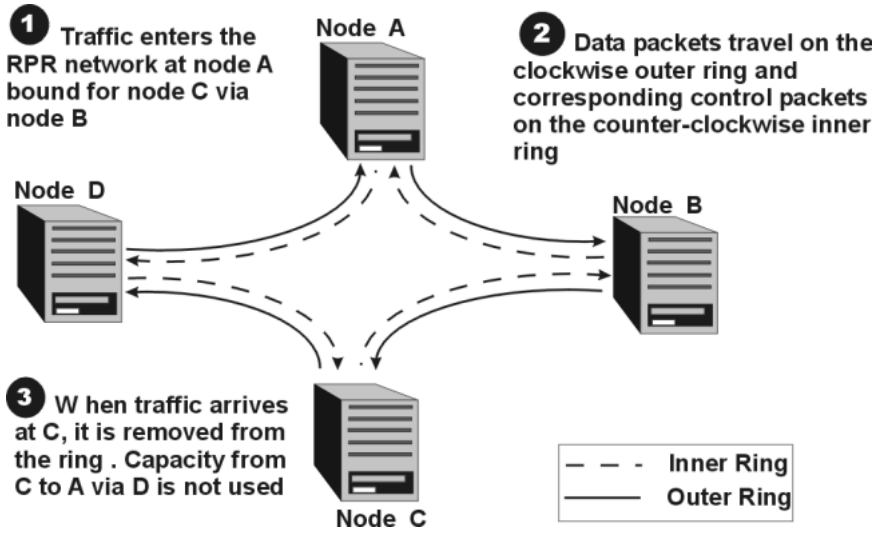

Figure 2.8: Basic Functioning of RPR

[FKY'00] and spatial reuse [CO'93]. In the case of the former, one RPR multicast packet is transmitted around the ring and can be received by multiple nodes. Mesh topologies require multicast packets to be replicated over all possible paths, wasting bandwidth. In the case of the latter, RPR unicast packets are stripped at their destination, allowing bandwidth to be used on multiple idle spans on the rings.

RPR packets can be transported over both SONET/SDH and Ethernet physical layers. The SONET/SDH physical layer offers robust error and performance monitoring. A robust Layer-1 protocol, SONET/SDH provides information such as loss of signal and signal degrade for use by the RPR protection mechanism. When using a SONET/SDH physical layer, RPR can be carried over SONET/SDH TDM transport or dark fiber. Ethernet provides an economical physical layer for RPR networks. RPR packets are transmitted with the required inter-packet gap. RPR systems (using the SONET/SDH physical layer) will not interoperate with Ethernet physical-layer-based systems on the same ring.

Protection of RPR rings

Two protection mechanisms have been defined for the RPR standard – steer and wrap. Both are required to guarantee sub-50 msec restoration time in the event

of a fiber cut or a node failure. Both can co-exist on an RPR ring, although only the steer mechanism is mandatory.

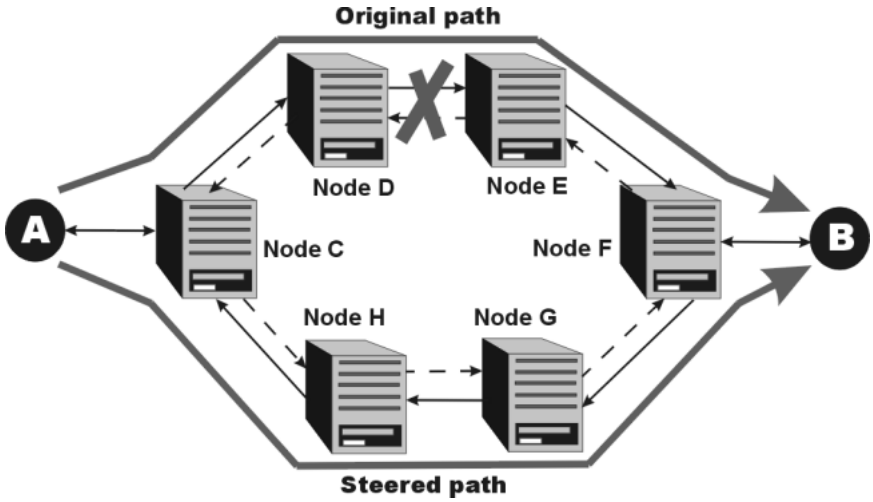

Figure 2.9: Steer Mechanism

Steer: Figure 2.9 illustrates the operation of the steer mechanism. In the event of a fiber cut or a station failure, the detecting station sends an indication message to all the stations on the ring. Stations that get the indication message steer only those flows, which are affected by the failure to their destination using the most suitable working portions of the ring.

The advantages of using the steer mechanism are: minimal delay on traffic during protection switching (flows are carried to their destination on the shortest available path), minimal re-ordering of packets during protection switching, and optimal bandwidth utilization (even during a protection event, the steer mechanism enables better-than-SONET bandwidth utilization). The limitations of the steer mechanism compared to the alternative wrap mechanism are higher packet loss during protection switching.

Wrap: Stations that use the wrap protection mechanism loop (or wrap) the signal upon failure detection. As illustrated in Figure 2.10, the connection is wrapped by the two stations closest to the failure.

The wrap mechanism is usually faster than the steer mechanism (although both guarantee sub-50 msec protection times) because rerouting is done locally, close to the failure. Packet loss during wrapping is minimal, it can be performed by hardware at the MAC level, and it is comparable to SONET's protection

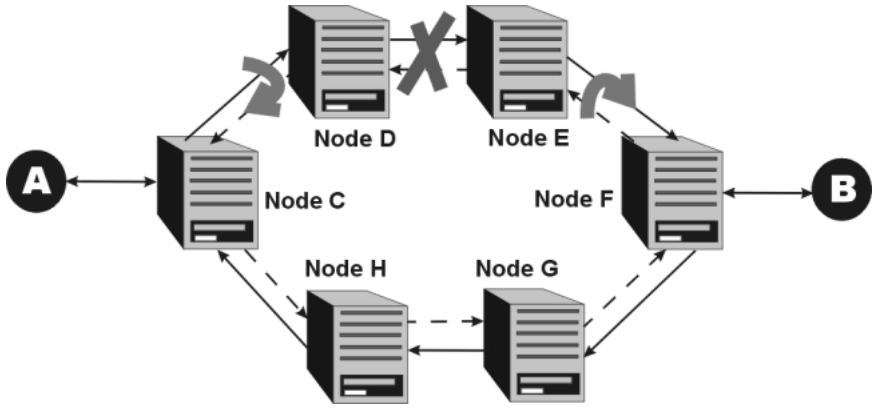

Figure 2.10: Wrap Mechanism

mechanism. The limitations of the wrap mechanism are relatively high delay for flows during wrap and less efficient bandwidth utilization (same-as-SONET) during protection events.

SWIS: The RPR MAC can use selective wrap independent steer (SWIS) as its resiliency method. The SWIS mechanism is the result of the recognition that both wrap and steer have their own advantages and limitations. Each of the methods can be desirable, depending on the type of traffic, and the carriers' requirements.

The SWIS mechanism enables co-existence of both protection mechanisms on the same ring, enabling an operator to choose the best protection mechanism per service; an operator who wishes to minimize packet loss during protection switching on a specific service will choose wrap as the preferred protection mechanism for that service. When minimizing jitter is important, steer will most probably be the preferred protection mechanism.

2.5.2 Metro Ethernet Network

Simplicity, robustness and cost-effectiveness have made Ethernet the most widely adopted LAN technology. Today standard compliant interfaces are running on a plethora of communication devices. The overwhelming majority of all data-transport starts and ends on an Ethernet LAN card. Ethernet became the dominant LAN technology during the 1990s. In 1999, more than 53 million ports of switched Ethernet were sold, making Ethernet one of the most popular utility interfaces next to the electrical outlet. Over 25 years ago, the inventors

of Ethernet could not have anticipated the tremendous impact and evolution of the protocol. The Institute of Electrical and Electronic Engineers (IEEE) has revised the protocol at least four times:

- from shared to switched
- from running over coax to running over fiber
- from known distance limitations to the possibility of being limitless, and
- from running at 10 Mbps to achieving 10 Gbps; all while maintaining its original frame format.

Carriers and service providers are addressing customer demand for simple and cost-effective Ethernet service (10 Mbps), Fast Ethernet service (100 Mbps) [QR'97], and Gigabit ethernet service (1000 Mbps) [CL'99] in the MAN and WAN. With the advent of Intelligent Optical Networking[2] and the advanced development of Ethernet, carriers/service providers can transform existing SONET/SDH infrastructures to offer end-to-end carrier-class Ethernet services. Intelligent, carrier-class Ethernet-over-optics services enable carriers to provide diverse bit rate services to customers cost-effectively.

Gigabit Ethernet over Metro Optical Network

The overwhelming popularity of Gigabit Ethernet (GbE) has made it the de facto standard for high-speed data communications in the corporate LAN environment. Within the traditional telecom infrastructure, however, access to Gigabit-level speeds to interconnect these LANs across the MAN or WAN is not only costly, but can take months to provision.

The compelling advantage of GbE in this architecture [San'02] is that it not only works efficiently with IP-based services, but it can also be used to create a single end-to-end IP network that can be implemented without the overhead cost and management complexity of traditional overlay transport networks. Since most user traffic starts from an Ethernet LAN and also ends at an Ethernet LAN, this architecture enables direct Ethernet connectivity (i.e. an Ethernet

[2]The recent advent of intelligent optical networking (ION) is playing a critical role in transforming the public network infrastructure by making it possible for service providers to deliver just-in-time bandwidth in both traditional TDM and emerging data formats. By combining the reliability and functionality of SONET/SDH, the capacity creation of DWDM and innovative IP-based networking functionality, ION is transforming the optical domain from a static transmission medium into a dynamic and agile infrastructure capable of supporting higher-layer services as well as a host of new value-added optical services.

port) between customer premises and service provider central offices, removing the need for costly and complex multiplexing or protocol conversions at the customer site.

And since IP and Ethernet are open and ubiquitous protocols, they facilitate the largest possible multiplicity of services and applications, while also enabling a completely new price/performance ratio compared with traditional telecom networks.

Protection

Protection mechanisms within Ethernet are extremely limited. This is because Ethernet had its origins in the LAN environment. The spanning tree algorithm [Per'92] handles link faults and often takes tens of seconds to converge for a large network. Ethernet's failure recovery time is far too high for voice, video and other mission-critical applications. This is in sharp contrast with a maximum recovery time of 50 ms via automatic protection switching (APS) in SONET/SDH.

The IEEE 802.1w [I802.1w] addresses the rate of convergence of the spanning tree algorithm by using the Rapid Reconfiguration of Spanning Tree protocol. However at a convergence rate of hundreds of milliseconds it is far slower than the 50 ms recovery time of SONET/SDH and is thus suitable for certain service classes.

2.6 The Case for Packet Ring Technology

Packet based technologies are increasingly gaining acceptance and importance due to the fact that data load is increasing more rapidly than voice. It is thus evolving from LANs to MANs. Ring is the most prevalent topology in the metro. However in section 2.3 we have explained how using SONET/SDH leads to bandwidth wastage. Ethernet on the other hand makes efficient use of bandwidth, as it is a packet-based technology. It has a wide base of infrastructure and thus it is ideal with respect to evolving into future networks. Advances in optical Ethernet technology now enable transmission at Gigabit speeds and is also optimized for IP traffic. In addition it has the advantages of being popular, simple and cost effective.

Thus, Ethernet does make efficient use of available bandwidth for data traffic, and does offer a far simpler and inexpensive solution for data traffic. However, it

also suffers from many disadvantages. Ethernet was originally designed for a bus (later on switched Ethernet made it possible to execute it over star topologies), and thus is not optimized for any other specific topology like rings. Ethernet does not take advantage of a ring topology to implement a fast protection mechanism. The inherent nature of Ethernet prevents it to work with loops. It thus makes use of the spanning tree protocol to eliminate all loops from a switched network. Even though the spanning tree protocol serves its purpose to achieve path redundancy in a simple manner, it recovers comparatively slowly from a fiber cut.

An additional drawback of Ethernet is related to fairness[3]. Fairness has never been easy for the mesh topology. However a ring is a much simpler topology and some control over traffic is possible. Once again since Ethernet does not take advantage of the ring topology it fails to provide fairness. Ethernet switches can provide link-level fairness, but this does not necessarily or easily translate into global fairness.

A Packet Ring technology combines the advantages of both Ethernet and SONET/SDH and thus provides the optimal solution for packet transport in the MAN. It is both a packet technology as well as optimized for rings. It thus combines efficiency, scalability, fast restoration and fairness. Packet Ring protocols create a full, packet-based networking solution that avoids the provisioning complications and inflexibility of SONET/SDH and provides the ring protection and global fairness features missing from Ethernet.

The basic advantage of a Packet Ring is that each node can assume that a packet sent on the ring will eventually reach its destination node regardless of which path around the ring has been taken. Since the nodes "know" they are on a ring, only three basic packet-handling actions are needed: insertion (adding a packet into the ring), forwarding (sending the packet onward), and dropping (taking the packet off the ring). This reduces the amount of work individual nodes have to do to communicate with each other, especially as compared with mesh networking where each node has to make a forwarding decision about which exit port to use for each packet.

Packet Rings have a natural resiliency advantage. A ring that is built using switches needs to distribute failure information across an entire network to recover fully from a fiber cut. In the Ethernet case, this can be accomplished using

[3]An access fairness protocol comprises of rules and behaviors to constrain access under certain conditions so as to ensure that geographically distributed nodes competing for the medium get a fair share of the medium.

a spanning tree protocol. On the other hand, a Packet Ring protocol can use a "ring wrap" at the nodes surrounding the cut. In this case, only nodes that are adjacent to the failure need to take any action. Wrapped traffic can reach the original destination by going around the ring in the opposite direction. Ring fail-over is often described as "self-healing" or "automatic recovery." In practice, ring-based transport systems have reliably achieved < 50 ms fail-over periods.

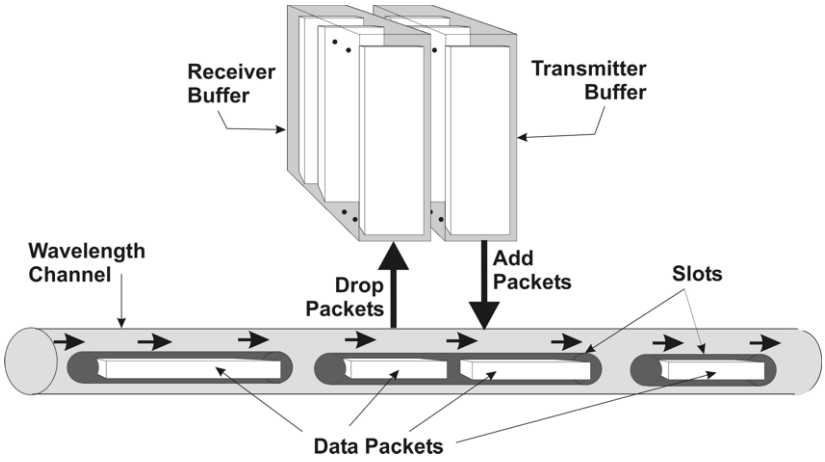

Figure 2.11: Concept of Time-slotting

2.7 Slotted Ring Network Architecture

Time slotting may be considered as one of the candidates in realizing an all-optical packet-switched ring network. Conceptually time-slotting is similar to TDM. In time-slotting each WDM channel consists of time slots, filled with data packets obtained from the higher networking layers. The concept of time-slotting is shown in Figure 2.11. Adjacent slots are separated from each other by an inter-slot gap. The receiver buffer removes data packets contained within the slots, and consequently the transmitter buffer adds new data packets to the slots. The size of the slots may or may not be fixed. Variable sized slots add to the MAC complexity. Depending on their sizes a slot may carry one or more data packets. Based on this approach, a number of network architectures have been proposed, some of which include [BA'02], [CEF'99] and [KPS'95].

2.7.1 Some Slotted Ring Architectures

Research in the area of WDM slotted-rings is not new. Three different concepts have been proposed by three different groups for transporting data-packets contained within slot over WDM rings.

Slotted Ring as proposed in [KPS'95]

The optical ring network consists of optical switching nodes linked by fiber optic cables to form a closed optical path. Each channel on the ring has a constant number of bit positions grouped into fixed-length slots circulating continuously around the ring. Each slot contains a bit in the header that indicates whether the slot is empty or in use. If the slot is empty it is available for use by a node. When a node receives an empty slot, the node captures the slot and transmits its cell in its transmit buffer. A destination node checks the address field of the received cell, removes the cell data from the cell, and makes the slot empty.

Slotted Rings based on the concept of HORNET

[BA'02] proposes a ring topology interconnecting nodes via a single unidirectional fiber. The bandwidth of the fiber is divided into multiple wavelength channels, which in turn are divided into fixed length time-slots, constituting a slotted WDM ring with data channels. Each network node is equipped with one tunable transmitter and one fixed-tuned receiver. The signaling information carried by the slot header on each channel is generated and detected by means of the subcarrier multiplexing technique. In HORNET each available wavelength channel is associated with a dedicated subcarrier frequency in order to provide and detect the slot availability status of all the channels and the corresponding destination addresses of transmitted packets. A small portion of the optical power is extracted from the ring for header processing.

Slotted Ring Architecture based on [CEF'99]

Nodes are grouped into S segment rings that are connected through bridges to a backbone ring. Bridges are conventional 2x2 space switches. Nodes are equipped with one tunable transmitter and one fixed receiver. Each node is also equipped with one fixed transmitter and one fixed receiver for signaling purposes.

If the number of data wavelengths $W \geq$ the number of nodes N in a segment ring then one reception wavelength is exclusively assigned to each node (assuming each node is equipped with only one fixed receiver). If the number of wavelengths is less than the number of nodes then N/W nodes share a given reception wavelength. The total bandwidth of each wavelength (including the signaling one) is divided into slots that rotate in the network and are statically allocated by network nodes. Information is removed from the network at the destination node enabling the reuse of the slot by other nodes. Transmissions traversing different links can therefore take place simultaneously thus providing higher throughputs and lower access delays.

The three architectures mentioned above do not provide any support for optical multicasting. Also they rely on the header contained within the slot to decide whether to switch the data packet contained in the slot. The FLAMINGO slotted-ring architecture is discussed next.

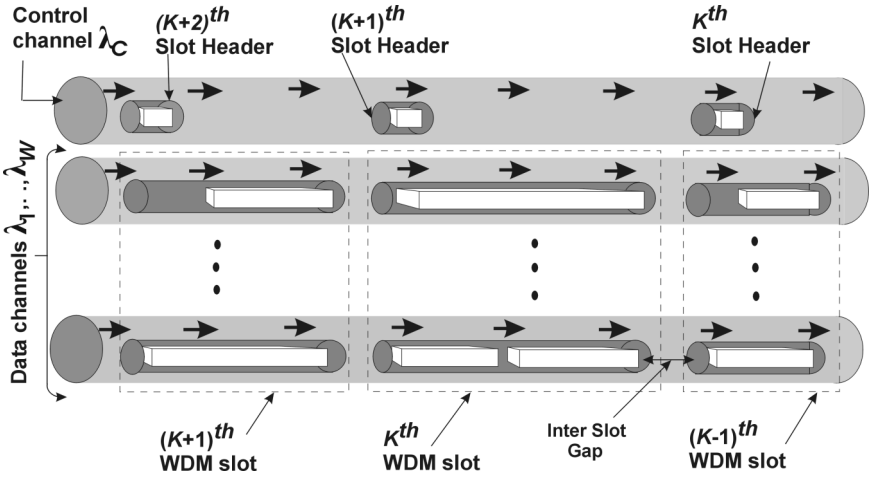

Figure 2.12: Synchronized WDM and Header Slots

2.7.2 Principles of operation and topology

In this thesis we consider a slotted multi-channel WDM network laid out as a ring. The ring comprises of dual counter-rotating fibers. [DBK+'01] analyzes a slotted-ring with a single fiber with slots rotating in one direction. Access to the ring is via nodes. Each of the WDM channels carries an equal and constant number of slots that circulate constantly around the ring. One of the

fibers transport the slots in the clockwise direction and the other in the counter-clockwise direction. Within each fiber corresponding slots on all the channels are assumed to be of the same size and are synchronized with each other to form a WDM-slot. This is indicated in Figure 2.12. This synchronization of slots across different wavelengths has been addressed in detail in section 3.2.1. Each slot on all of the WDM channels but one carries one optical data packet, whereas the last remaining channel is used to transport control information. We will refer to slots on the control channel as slot headers since they carry control information to all of the data slots that constitute a particular WDM-slot. As a result, the total bandwidth of the optical fiber is split in two dimensions: optical frequency, due to the presence of multiple WDM channels and time, due to time-slotting. This provides the basis for an efficient multiple access mechanism since total bandwidth of the system happens to be more finely divided in comparison with pure WDM networks. Also, as compared to TDM networks, the concept of time-slotting enables efficient transport of data traffic. At any given moment in time, a large number of users can carry out their communication sessions, which is considered a valuable property as far as LANs and MANs are concerned.

Transmission of data packets and slot headers on different wavelength channels separates the data (fed in by the upper layers and transported through the optical layer in all-optical fashion all the way from the source node to the destination) from the control information, which requires electronic processing in the intermediate nodes. Such separation makes the network transparent with respect to data transmission bit rates and protocols, which is seen as another important benefit of the described architecture.

Communication between network nodes through WDM-slots can be described as follows. When a WDM-slot arrives at a node, its header is optically dropped (demultiplexed) from the WDM signal and fed into a photodetector. The information contained in the slot header fully describes the destination and status (full/empty) of each data slot within the corresponding WDM-slot. Based on this information the decision is made by the control unit as to which of the data slots within the WDM-slot are destined to the node and therefore must be dropped and to which of the data slots the node is allowed to insert its own data packets. Since processing of the slot header and reconfiguring the optical components takes time, the data slots must be delayed by an optical delay line. The basic schematic of the add and the drop functionality is shown in Figure 2.13. This dropping of a data packet at its destination node and allowing insertion of another data packet at the same node enables spatial reuse

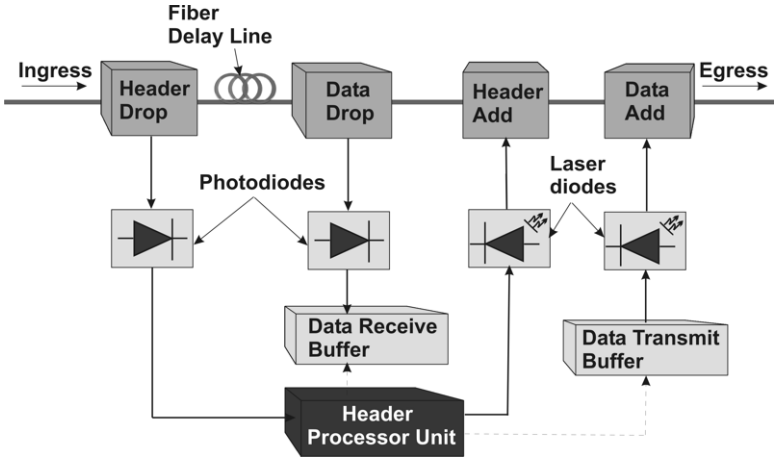

Figure 2.13: Schematics of the ADD/DROP functionality

of the ring's network resources.

One of the nodes on the ring acts as the central network controller. Among other jobs the central network controller has the functionality of informing nodes on the ring about failures. At the MAC layer the central network controller could have the function of allocating transmission quotas to nodes. The central network controller and its functions are beyond the scope of this thesis.

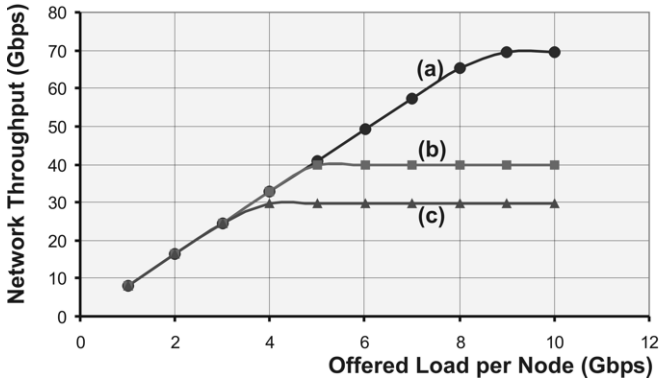

Figure 2.14: Network Throughput comparison: (a) Transmitter and Receiver Arrays; (b) Receiver Array and Fixed Transmitter; and, (c) Transmitter Array and Fixed Receiver at all nodes

For adding and dropping data packets, the nodes can have one of the following three capabilities:

- Each node is able to receive at any one wavelength and transmit at all wavelengths on the ring;
- Each node is able to transmit at any one wavelength and receive at all wavelengths on the ring [DKS'00]; and,
- Each node is able to transmit and receive at all wavelengths on the ring [DKG+'01].

By transmitting and receiving at all wavelengths we imply transmitter and receiver arrays. Tunable transmitters are not considered because a tunable transmitter is limited by its ability to transmit only on one wavelength at any instant of time. This implies severe wastage of bandwidth as only one empty slot on one particular wavelength within a WDM slot, containing empty slots on other wavelengths, can be filled. The first two cases provide cost benefits per node due to the fewer number of transmitters or receivers involved as compared to the third case. The difference between the above three cases can be understood when we think in terms of traffic performance. Suppose that the throughput of a node is defined as the rate at which packets leave the node buffer under stability conditions (that is packet arrival rate is less than the rate at which packets depart). Also, suppose that slot-utilization is defined as the average utilization of all slots observed at the instant a slot departs a node. Under these definitions it is obvious that a node with the ability to receive and transmit at any wavelength will outperform the other two cases.

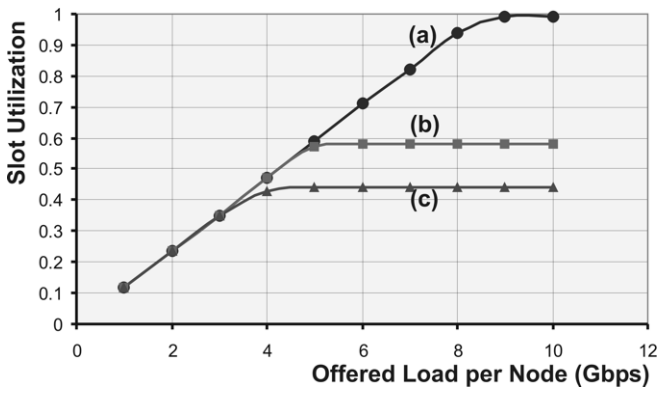

Figure 2.15: Slot Utilization comparison: (a) Transmitter and Receiver Arrays; (b) Fixed Transmitter and Receiver Array; and, (c) Transmitter Array and Fixed Receiver at all nodes

We simulated the above three cases in C++ under the following assumptions. The network was assumed to be a bidirectional ring with two counter-rotating fibers transporting slots of size 500 bytes and separated by 2 bytes. There were 8 nodes on the ring separated by 20 km of fiber. Each fiber was carrying 4 WDM data channels, each at 2.5 Gbps. The arrival process at each of these nodes was similar and comprised of fixed size data packets (500 bytes, and thus equal to the slot-size) arriving according to a homogeneous Poisson Process with rate λ. Upon arriving at a node, a data packet is inserted into a finite buffer. At the node data packets are put onto passing empty slots only if the direction of travel (clockwise or counter-clockwise) of the slot ensures that the packet reaches its destination via the shortest path (shortest in the sense of the number of traversed nodes). Thus in both directions, clockwise and counter-clockwise, there are a maximum of three intermediate nodes for a connection with the longest reach on the ring. In the case of transmitter array and fixed receiver we had to allocate quotas to the nodes to send packets on each wavelength. This is because since the receivers are fixed a slot can only be sent to a particular node. In our simulation the number of nodes is exactly twice the number of wavelengths. If we assume that nodes able to receive at the same wavelength are diagonally opposite to each other, then a slot arriving at a node to be received will be used to send data to its diagonally opposite node. Soon slots will be monopolized on the ring. To avoid this situation we had to adopt the quota system. The use of quotas is to obtain simulation results under the simplest of conditions and is no way related to the MAC.

The results are presented in the plots of figures 2.14 and 2.15. First we analyze the case in which all nodes are able to transmit and receive at all wavelengths. A destination node, which is only one hop away from its source, can be reached in one way. Since the destination node's relative position can be two possibilities, namely clockwise and counter-clockwise, we have the following probabilities:

P(reaching a node one hop from its source) = 2/7;

P(reaching a node two hops from its source) = 2/7;

P(reaching a node three hops from its source) = 2/7; and,

P(reaching a node four hops from its source) = 1/7; this can be reached either clockwise or counter-clockwise.

$\Rightarrow$ Average distance traveled by a slot $= [\frac{2}{7} \times 1] + [\frac{2}{7} \times 2] + [\frac{2}{7} \times 3] + [\frac{1}{7} \times 4] = \frac{16}{7}$ nodes.

Since we have a bi-directional ring each of 4 wavelengths at 2.5 Gbps, we

have an installed capacity of $2 \times 4 \times 2.5 = 20$ Gbps.

$\Rightarrow$ Maximum throughput the network can support $= 20 \times \left(\frac{8}{16/7}\right) = 70$ Gbps.

This is observed in figure 2.14. At this stage the slot utilization must be close to 100%, which is observed in figure 2.15. In the case that a node is able to transmit at only one wavelength and receive at any wavelength we have two nodes diagonally opposite to each other which can transmit at the same wavelength. This implies that the slot can actually serve exactly twice in one rotation around the ring, implying a distance traveled by the slot equal to 4 nodes.

$\Rightarrow$ Maximum throughput the network can support $= 20 \times \left(\frac{8}{4}\right) = 40$ Gbps.

This can be observed in figure 2.14. This drop in throughput of approximately 43% is also observed in the slot utilization of figure 2.15.

The last case (transmit at any wavelength and receive at only one wavelength) is very similar to the previous case in that a slot is able to serve exactly twice in one revolution around the ring, which should theoretically lead to a maximum throughput of 40 Gbps. However the graph indicates a maximum throughput of 32 Gbps. This is probably as a result of allocating quotas.

Thus we see that when all nodes are equipped with transmitter and receiver arrays we have a far better performance. The added advantage of using arrays of transmitters and receivers is that in the event of a failure of a single transmitter or receiver the node is not cut-off from the ring. We assume that this advantage coupled with the performance benefits outweighs the cost implications of having multiple receivers and transmitters per node. Henceforth, throughout our discussion we assume that the node uses transmitter and receiver arrays to be able to transmit and receive at all wavelengths on the ring.

2.7.3 Enabling Multicasting in the Physical Layer

WDM has dramatically increased the capacity of point-to-point links. This has resulted in the creation of opaque optical networks in which the optical signal undergoes conversion into the electronic domain and back at every intermediate node. As more and more all-optical cross-connects are becoming available, designing and deploying transparent networks are steadily gaining popularity. In such a network a lightpath starts at a source node and ends at a destination node spanning a number of intermediate nodes and links. [SM'99] extends the concept of light-path to light trees, the difference being that the latter has multiple destination nodes. Figure 2.16 shows the picture of a light-tree. Light-

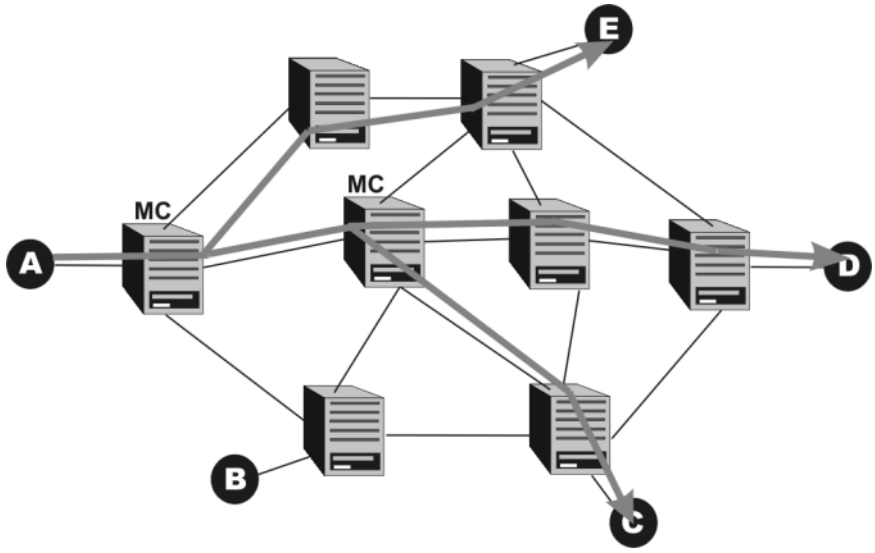

Figure 2.16: Light Tree in a Mesh topology. Nodes labeled MC are Multicast Capable in the optical domain

trees may be implemented by usage of optical power splitters at the nodes. An advantage of using a light-tree is optical multicasting which otherwise requires opto-electronic conversion. This extension of multicast capability to the optical domain provides

- Performance Enhancement: increases network throughput owing to lesser link utilization and more efficient bandwidth usage;
- Connectivity Improvement: enhances the virtual connectivity of a network;
- Cost Reduction: reduces usage of optical hardware (e.g., transceivers);
- Meshed Protection: efficient implementation of the 1+1 protection possible if the primary and back-up paths are part of a light-tree rooted at the ingress MC of figure 2.16;
- Ring Interconnection: especially beneficial for ring topologies where a connection can drop a packet and continue to the next downstream node to drop the same packet and so on.
- Traffic Grooming: grooming of LSPs in Generalized multiprotocol label

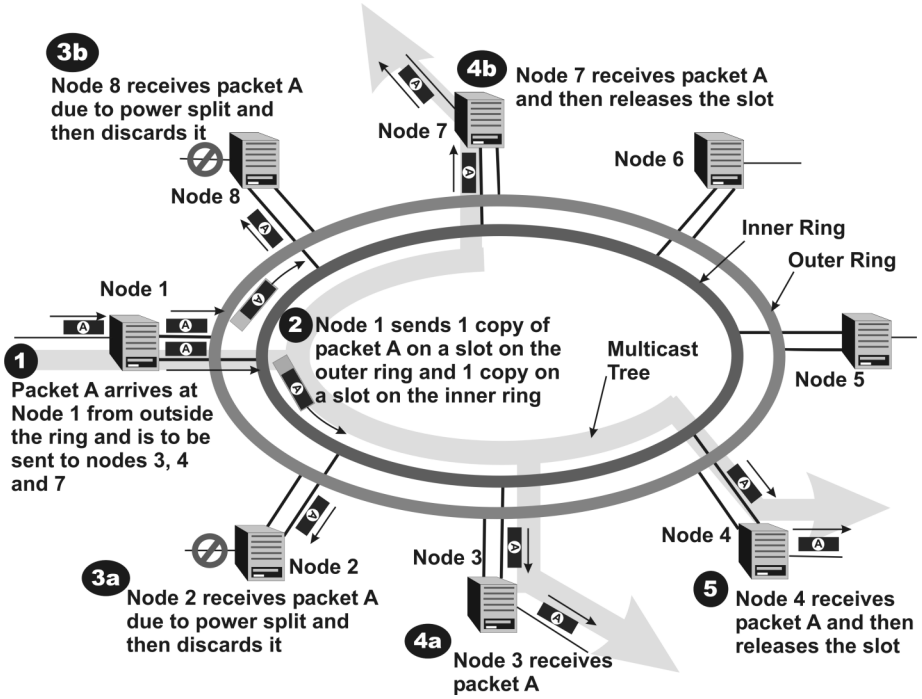

Figure 2.17: Multicasting in the Slotted Ring Network. To be read in the order 1, 2, 3(a,b), 4(a,b), 5.

switching (GMPLS[4]). For further reading on GMPLS the reader is referred to [IETF02].

The power splitter provides the basic functionality for realizing multicast at the optical layer. It is a passive device splitting the power of an optical signal. A N-way power splitter divides input signal power between N outputs reducing input power theoretically by a factor called the splitting ratio. Splitters can be static and dynamic as well. The former provides single and constant power splitting ratio whereas the latter provides dynamic control of the power splitting ratio providing a discrete set of capabilities. One of the greatest drawbacks of such a approach lies in itself, namely the splitting of power. This leads to loss and often require more amplifiers and more amplifiers imply SNR degradation.

[4]Generalized MPLS (GMPLS) extends MPLS to provide the control plane (signaling and routing) for devices that switch in any of these domains: packet, time, wavelength, and fiber. This common control plane promises to simplify network operation and management by automating end-to-end provisioning of connections, managing network resources, and providing the level of QoS that is expected in the new, sophisticated applications.

Therefore care must be taken in using power splitters and also the amount of power being split at them.

In the slotted-ring network discussed in 2.7.2, we propose the usage of splitters at all the nodes on the ring to split the power of all the data channels [DBK+'01b]. Part of the power is always dropped for receiving the data. The received data is then rejected or accepted based on the destination information contained in the slot-header. The remaining optical power passes on to the downstream node. This way all the nodes are multicast capable. The last destination node takes off the data packet and releases the slot for re-use. Figure 2.17 shows a multicast tree in the slotted ring that is under consideration. For protocols supporting IP multicasting in all-optical slotted-ring networks, such as the one under consideration refer [SGD'01b]. For further reading on supporting IP multicasting in WDM all-optical networks in general please refer [SGD'00], [SGD'01c] and [SGD'01].

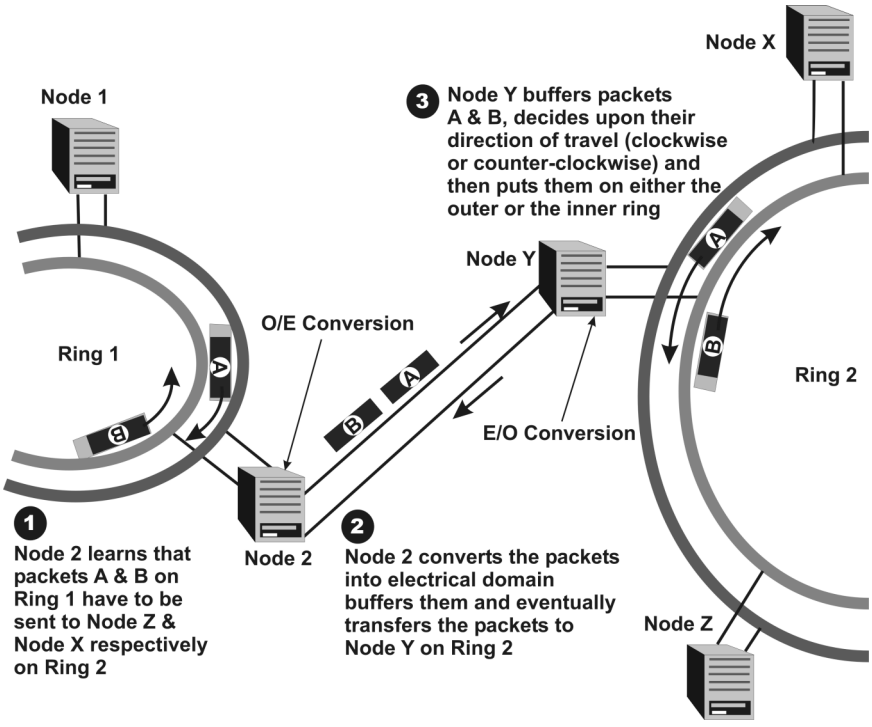

Figure 2.18: Interconnected Slotted Rings

2.7.4 Interconnected Slotted Rings

To enable scalability and to increase geographical reach, it is practical to have a network with interconnected rings. The rings function independent of each other. Figure 2.18 shows interconnected slotted rings with the steps involved in packet transfer from one ring to the other. A ring may be connected to an adjacent ring at more than one point. A failure on any one ring is thus localized on that ring and does not bring down the whole network. Each ring has dual counter-rotating fibers. Also, each ring has its own set of slots that do not cross over from one ring to the other. In traveling from one ring to another a data packet undergoes conversion into the electronic domain and back to the optical domain. This is because the packets have to be buffered till an empty slot (on the next ring in its path) comes by. The slot headers corresponding to these buffered packets are also buffered. When an empty slot passes by, a buffered packet is put onto it and its corresponding slot header is also copied onto the slot header of the passing slot. The number of slots in a ring may vary depending upon the ring's size. The number of wavelengths on a ring may differ from any other ring interconnected to it. Also the bit rate per wavelength on a ring may vary between rings.

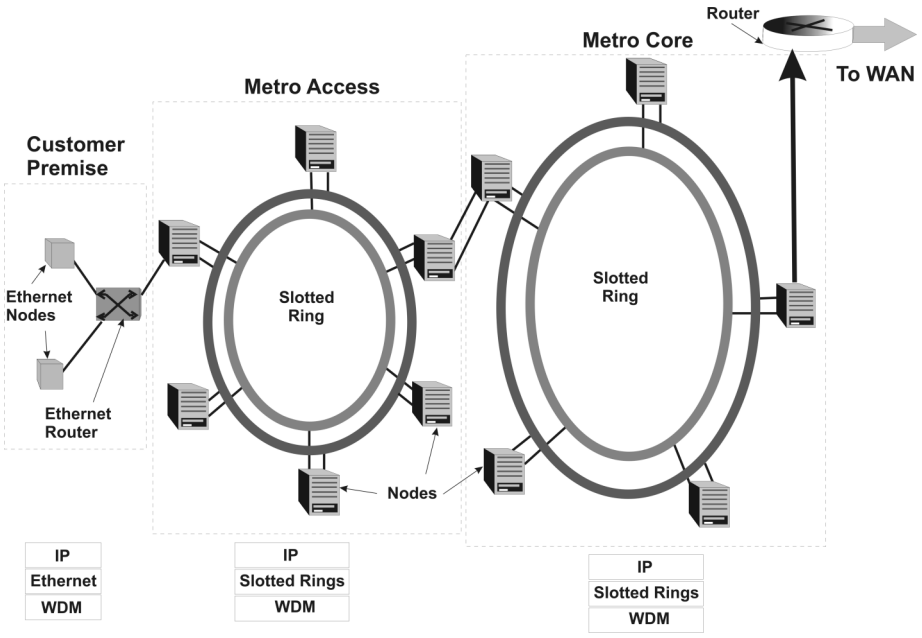

Figure 2.19: Overview of the Network and the Layers

The rings can be interconnected such that there exists one core ring in the MAN connected with access rings in the way as indicated in figure 2.18. The core ring may have a higher capacity than the access rings. The access rings in turn are connected to enterprise networks. Figure 2.19 depicts an overview of the network layers beginning from the enterprise LAN through the metro access and core to the WAN. In the enterprise networks Ethernet is the dominant LAN technology. IP packets are transported over Ethernet over the optical network. On departing the LAN the IP packets are stripped off and are handed over by the ethernet router to a node on the slotted access ring. The IP packets are then transported in slots over the slotted ring access and core rings.

2.8 Concluding Remarks

The use of a ring-based interconnected network in the MAN space provides numerous advantages, including: (1) there is a unique path between any two points on the network, so that the ordering of packets is always maintained, (2) information can be sent from one point in the network to one or more other points, providing a natural multicast mechanism, and (3) a simple routing scheme can be used, allowing for high-speed operation of the rings and (4) takes advantage of existing ring-based infrastructure in the MANs. For any multicast connection there exists at most two branches, separated at the source. One of them is clockwise and the other counter-clockwise.

The concept of transporting packets using slots enable IP packets to be transported over WDM with relative ease. It preserves the data packets in the optical domain enabling bit-rate and protocol transparencies. It is also possible to support all-optical multicasting. In this thesis no reference to the related MAC of the slotted-ring is made. For reading on the MAC the reader is referred to [SGD'02] and [SGD'02b]. In the following chapter we discuss the architecture of the node, which supports these requirements and more to enable the creation of an all-optical ring.

CHAPTER 3

Node Architecture

3.1 Introduction

The vital elements of any network are its nodes. The node allows access to the network and it performs traffic routing functions. It makes decisions based on network and traffic parameters and information available at the MAC layer. This thesis is devoted to ring-shaped metro networks where add/drop nodes are the access points to add/drop packets to or from the ring. Often, apart from simply adding/dropping data packets it has to perform other sets of functions. These functions may range from wavelength conversion, amplification and protection functions (such as ring wrapping) at the physical layer to altering information contained within packet headers. It may do all of these and more functions partly or wholly in the optical domain. Doing these in the optical domain has the advantages of bit-rate and protocol transparencies, making capacity upgrading and network scaling easier. Technological limitations often prohibit these functions being performed completely in the optical domain. In such an eventuality, the data needs to be converted into the electronic domain and back. This implies introducing optical delay lines and/or electronic buffering at the nodes. For example, buffering is needed for contention avoidance.

In section 3.2, the issues that need to be taken into account when designing the architecture of the node are first identified. These issues arise either from the propagation of light in standard single mode fiber and other optical devices (such as wavelength-selective elements, optical switches and optical amplifiers) or from requirements imposed by the network architecture proposed in chapter 2 and from traffic characteristics to be handled. In section 3.3 we present the types of node architectures prevalent in present-day optical networks. Subsequently, a block diagram of the node and its functions is presented in section 3.4. Sections 3.5 to 3.11 discuss the components and devices that are best suited for the architecture of the network presented in chapter 2. Finally the complete architecture of the node is presented in section 3.12.

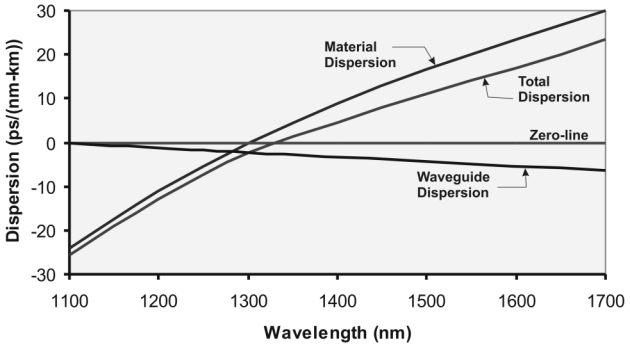

Figure 3.1: Dispersion in Standard Single Mode Fiber as function of Wavelength

3.2 System Design Issues

The design of a node is one of the factors that determines the physical layer performance of the network. The physical layer performance issues range from parameters such as crosstalk and SNR to chromatic dispersion and polarization. Therefore, before starting to define and build the node architecture it is of paramount importance to investigate the issues/problems that may arise during the operation of the network. Issues imposing design constraints on the node architecture can be broadly divided into two categories. Some issues may arise from the inherent nature of the slotted ring network architecture (proposed in chapter 2), and thus are very network-design specific. Function specific issues may arise from the functions that the network has to perform. Network-design

specific issues may include noise accumulation, crosstalk, wavelength conversion, power loss and dispersion. On the other hand, function specific issues are mainly imposed by traffic characteristics and may include the inter-packet (slot) gap (figure 2.12), which has a direct implication on the switching delay and packet-header (slot-header) processing delay, which affects the length of an optical delay line. Some issues that have to be considered when designing the node are discussed next.

3.2.1 Slot Synchronization

As a signal, which is not purely monochromatic, travels down the length of the fiber it experiences broadening. This broadening is called Chromatic Dispersion. Mathematically it is related to the second derivative of optical phase with respect to frequency, group delay being the first. Chromatic Dispersion consists of two components: material dispersion and waveguide dispersion. Material dispersion is the dominant source of dispersion in standard single-mode fibers. Figure 3.1 shows chromatic dispersion and its components in standard single-mode fiber as a function of wavelength.

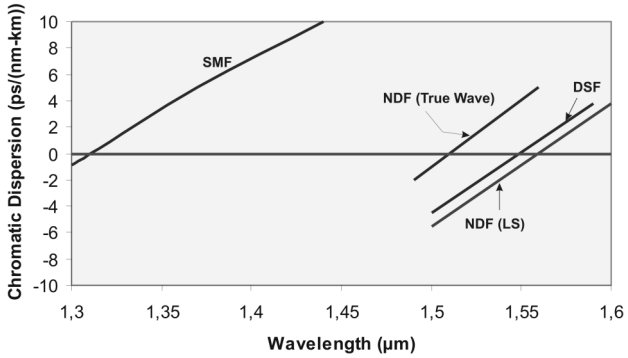

Figure 3.2: Chromatic Dispersion in Fibers as function of Wavelength; SMF: Single Mode Fiber; DSF: Dispersion Shifted Fiber; NDF: Normal Dispersion Fiber

Chromatic dispersion is attributed to the finite spectral width of optical signals because different spectral components propagate at different speeds along the length of a fiber. This velocity difference is due to the difference in effective refractive index of the fiber for different wavelengths and is termed material and waveguide dispersion. Figure 3.2 shows the variation of chromatic dispersion

with wavelength in different types of fiber. This difference is mainly attributed to waveguide dispersion.

Chromatic Dispersion can lead to higher bit error rates (BERs) in digital communications if not compensated. Pre-chirping of laser pulses [NYT'00], the use of dispersion-compensating fibers [VR'93], optical phase-conjugation [WNC'93], and optical filters (such as cascaded Mach-Zehnder interferometers [CDR'95], and fiber gratings [EBT'94]) are techniques to compensate for chromatic dispersion.

In the slotted ring network proposed in chapter 2 and in figure 2.12 it has been explained that one of the fundamental concepts behind the operation of the network is that all slots contained within a WDM-slot must arrive at and depart a node all at the same time. The WDM-slot must be aligned with its corresponding slot header. Based on the information contained within the header slot, slots within the WDM-slot are either dropped or added. Because of chromatic dispersion, these slots will lose their mutual alignment. As a matter of fact, in the absence of any correction mechanism the misalignment will accumulate with increasing path-length in the ring.

3.2.2 Optical Multicasting

Multicasting in the optical domain can be achieved by the use of power splitters. Part of the power is dropped for receiving and the remaining power is allowed to pass through. A splitting ratio that enables a higher power to be dropped weakens the optical signal that has to pass through to downstream nodes considerably. This can be compensated by amplifiers. However amplifiers degrade SNR. On the other hand, a splitting ratio that enables lower power at the receiver will raise the BER. Therefore the splitting ratio must be well-chosen to increase the reach on a ring and also to keep the BER below an acceptable limit.

Using power splitters at a node has another major disadvantage. Suppose we have a WDM system with W channels. If the data contained in $\tilde{W}(< W)$ channels is to be multicast at a node then we have to split power on these $\tilde{W}$ channels. This implies that depending on the splitting ratio the powers of $W - \tilde{W}$ channels may be considerably higher than the $\tilde{W}$ channels. In WDM networks channel powers must remain roughly the same, that is, the systems ideally should have no spectral ripple. A system with no spectral ripple has a flat power spectral density across its operating bandwidth. The problems of a system with a lot of spectral ripple are concentrated at the amplifier. An amplifier, such

as the EDFA with power and wavelength dependent gain characteristics will lead to SNR degradation if the power levels of the channels are substantially unequal [Kei'99]. Several dynamic gain equalizers have been demonstrated ([YLK+'99], [OHB+'00]). However, system designers aim at maintaining equal power levels across all the channels of a WDM system. Using gain-equalizers lead to unequal SNRs across WDM-channels.

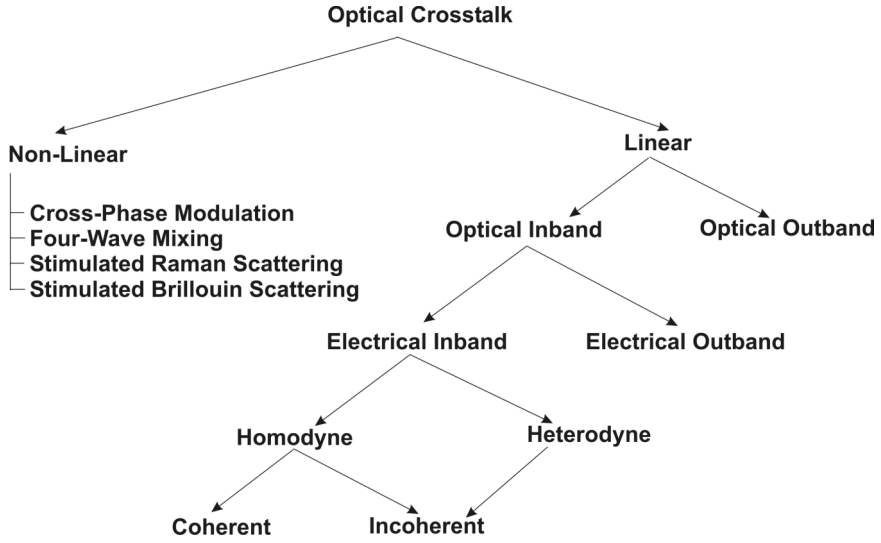

Figure 3.3: Overview of different types of Crosstalk in WDM systems, adapted from [Tan'01]

We propose to split all the data channels of figure 2.12. This helps maintain the power level of all channels at the same level and leads to equal SNR degradation after optical gain. Also it implies less delays at a node. Requesting a node to ascertain which of the W data channels are to be multicast and then using active elements to drop power from those channels implies more processing and network element reconfiguration and thus greater delays.

3.2.3 Crosstalk

Crosstalk is one of the most important issues in the design of WDM networks. It leads to the degradation of system performance when the power from one channel affects the power of another channel. Crosstalk can be classified in many ways. Broadly they fall in two categories: linear and non-linear. Figure 3.3 presents an overview of the different types of crosstalk.

Non-linear crosstalk arises due to non-linear effects in optical fiber. In the presence of high optical powers the refractive index of a fiber depends on the signal-intensity propagating in the fiber [Chr'90]. Intensity modulation being the most used modulation technique in fiber-optic networks, the intensity of a signal varies in a fiber. This variation causes changes in the refractive index of the fiber, which in turn leads to phase variations on other channels present in a WDM link. This gives rise to crosstalk of the type cross-phase modulation [KSS'97] and four-wave mixing [Ino'92]. The non-linearities also give rise to scattering effects when lightwaves interact with vibrations of silica molecules (leading to stimulated Raman scattering [GS'93]) and with acoustical waves (leading to stimulated Brillouin scattering [MR'92]).

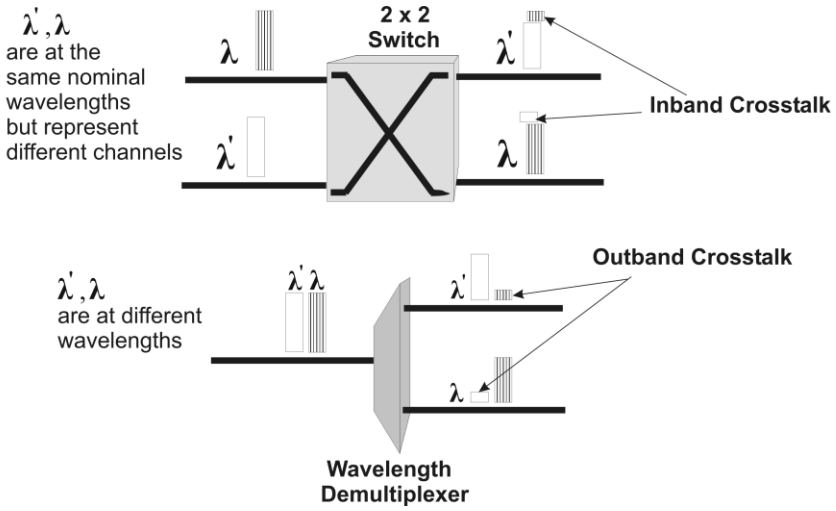

Figure 3.4: Inband and Outband Crosstalk

Linear Crosstalk arises because of the imperfect nature of WDM components such as multiplexers, demulitplexers and switches. Linear Crosstalk has been extensively studied in [BCL'97] and [BGT'96]. Linear crosstalk can be classified as optical inband or optical outband, depending upon its spectral location with regards to the passband of a filter. In a WDM system, outband crosstalk arises from channels at different wavelengths. This type of crosstalk can be easily suppressed by using a narrowband optical filter. Optical inband crosstalk arises when a signal and interferers have wavelengths that are so close to each other that they pass through the passband of a filter. This type of crosstalk causes severe degradation in the receiver system performance. Once generated it is

impossible to remove optical inband crosstalk. Optical inband crosstalk can be further classified based on the electrical spectral difference between an optical signal and crosstalk. If the difference is less than the electrical bandwidth of an optical receiver, then it is electrical inband crosstalk else it is electrical outband crosstalk. Electrical inband crosstalk can further be classified into homodyne and heterodyne crosstalk. Homodyne crosstalk occurs when a desired signal and crosstalk in the electrical domain have the same nominal frequencies. If the signal and crosstalk have closely-valued frequencies the crosstalk is said to be heterodyne. Homodyne crosstalk is either coherent or incoherent. If signal mixing happens within the coherence length of the laser, then it is coherent, else it is incoherent. In the remainder of this thesis the term inband crosstalk is used to indicate optical crosstalk, whose beat power is largely inside the electrical bandwidth of an optical receiver.

3.2.4 Power Budget

The system power budget [Agr'97], is the difference of the transmitter output power, augmented by optical amplifier gains, and the minimum needed receiver input power. It is calculated to obtain the allowed network losses (splitting loss, fiber loss, etc.) and its degradations. Based on the power budget calculations, decisions are made about amplifier placements in the network. Decisions are also made about splitting ratios at optical power splitters in the event of optical multicasting. In power budget calculations usually five main parameters are involved. These include the average launch power of the transmitters, P_{Tx}, the receiver sensitivity, P_{Rx}, the total channel loss, L_C, the system margin, M_S and the amplifier gain, G. The receiver sensitivity is defined as the minimum average received power required by the receiver to operate at a given BER. The system margin takes care of additional sources of power penalty that develop during system lifetime. Usually a system margin of $6 - 8$ dB is allocated during design. The channel loss takes into account loss of power experienced by a channel from the transmitter to the receiver, including splice and connector losses. These five quantities when expressed in decibels (dBm and dB) must follow the following relation:

$$P_{Tx} = P_{Rx} + L_C + M_S - G.$$

3.2.5 Timing Issues

One of the consequences of the slotted-ring network presented in chapter 2 is that the slot headers have to be electronically processed. Based on the information contained within the slot headers, control signals are generated on completion of processing. These control signals reconfigure and/or activate network elements such as switches, transmitters and others. The related time-durations, needed for the slot header processing, have direct impact on the inter-slot gap (see figure 2.12) and on the length of the fiber delay line (shown in figure 2.13) that has to be introduced to accurately delay a WDM slot.

3.3 Optical Node Architectures

Optical Nodes in today's networks can be broadly divided into two types: OXCs and OADMs. This classification is mainly functional. OXCs are the cornerstone of photonic layer providing network operators with added flexibility over the network architecture and survivability by switching in the space and wavelength domains. OADMs on the other hand perform add-drop operations at the wavelength level. In the paragraphs that follow OXCs are briefly discussed and OADMs are considered in detail. OXCs are popular in mesh topologies where multiple paths are possible. In the case of an optical ring, such as the one described in chapter 2, nodes are functionally similar to OADMs.

3.3.1 Optical Cross Connects

The main function of the OXC is to dynamically reconfigure the network in the wavelength and space domains to accommodate changes in traffic/bandwidth demand, to alter optical paths and to assist in restoration in the event of failures. Chronologically speaking, OXCs can be put in two broad classes, static and dynamic. A static OXC, which is obsolete provides a static interconnection of wavelength and space channels at input and output ports. It is based on a passive wavelength multiplexer/demultiplexer, for example an arrayed waveguide grating (AWG). The lightpaths from an input port to an output port were static. A dynamic OXC comes with a switch core capable of shifting lightpaths from any wavelength channel at any input port to any output port. They can support circuit-switching, burst-switching and sometimes even packet switching. There are two main types of dynamic OXCs: with wavelength conversion

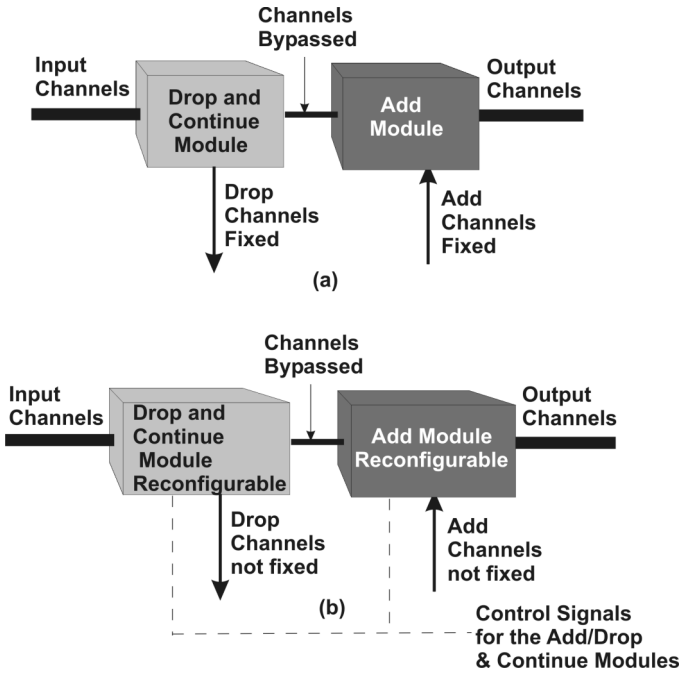

Figure 3.5: (a) Fixed and (b) Reconfigurable OADM

to reduce contention and without wavelength conversion. For a detailed study of these types refer to [MS'01]. The heart of a dynamic OXC is its underlying switch fabric. The switch fabric may either have an electrical core or an optical one. Economical limitations have until now prevented the use of OXCs with an optical core in commercial networks.

3.3.2 Optical Add Drop Multiplexers

The function of an OADM in an optical network is to drop and add one or more wavelength channels at a specific site in the network. Wavelengths within the same incoming fiber that need not be dropped should pass through to the output of the OADM. Broadly speaking, its job is to enable access to the optical bandwidth. OADMs have evolved over the years. Each generation has its benefits and drawbacks. OADMs can be broadly classified as fixed and reconfigurable. Figure 3.5 shows their principal difference.

Fixed OADMs

This is the simplest type of OADM, in that the wavelengths to be dropped and added are pre-specified. They are simple, protocol independent, bit-rate transparent and low cost. Network management in this case is limited to monitoring defects. However because of their fixed nature a significant amount of planning is required to specify the add/drop wavelengths at each OADM. Fixed OADMs are increasingly becoming obsolete.

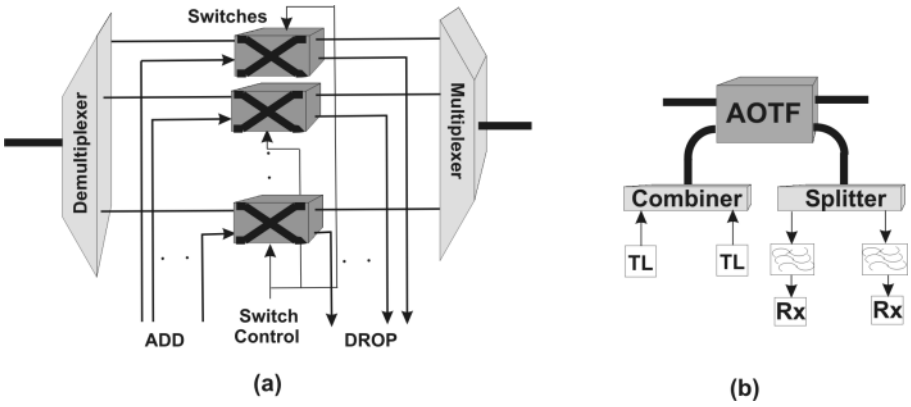

Figure 3.6: Examples of ROADM using (a) 2x2 switches and (b) using Acousto-Optic Tunable Filters (AOTF) and Tunable Lasers (TL)

Reconfigurable OADMs

Reconfigurable OADMs (ROADM) is an emerging generation of OADMs. Most of them have passed field trials and are currently in the process of consideration for deployment. This class of OADMs enable a selectable set of wavelength channels to be dropped/added at any site. The switches can be MEMS (Micro Electro Mechanical Switches)- based, electro optical, acousto optical, bubble jet, semiconductor optical amplifier (SOA) gates or liquid crystal-based. Among these, electro-optical switches (e.g. lithium niobate ones) combine speed with maturity. The system is easily scalable to higher channel counts at the expense of more complex WDM devices. They are easy to provision and the reconfiguration can be done per packet basis if the switches are fast enough. However configurable OADMs because of their inherent architecture are usually characterized by high insertion losses (with the exception of MEMS). The ROADM market is now witnessing a range of technologies in which every conceivable

filtering and switching technology is being proposed for ROADM use. Figure 3.6 depicts two examples of ROADMs. Table 3.1 below compares the two types of OADMs.

Type	Fixed OADM	ROADM
Add/Drop Wavelength	Fixed	Variable (Circuit Switching, Packet Switching)
Number of Dropped Wavelengths	Fixed	Variable
Key Devices	Fiber Grating Dielectric Filter	Optical Switch, Wavelength Demultiplexers
Network Management	None	Considerable
Planning	Significant prior to deployment	None
Traffic	Not Optimized for dynamic traffic	Optimized for dynamic traffic
Cost	Inexpensive	Very expensive

Table 3.1: Comparison of OADM types

The RINGO Node

The concept of Ringo [GCF+'01] uses an all-optical ring with tunable transmitters and fixed receivers. Each node receives packet on a single wavelength but can put packets on the ring at any wavelength. The number of nodes on the ring is equal to the number of wavelengths. Fixed wavelength add-drop filters at the receiver drop the required wavelength. This is shown in figure 3.7. Packet collision is avoided at the transmitter using an empty-slot strategy based on carrier-sensing (CSMA). In such an architecture flexibility and scalability are central issues. Also if there is no packet to be sent to a node, bandwidth on its corresponding receiving wavelength is wasted. In the event of a fault on this particular wavelength, protection is either difficult or involves over-capacity provisioning. Also optical multicasting is impossible with such an architecture.

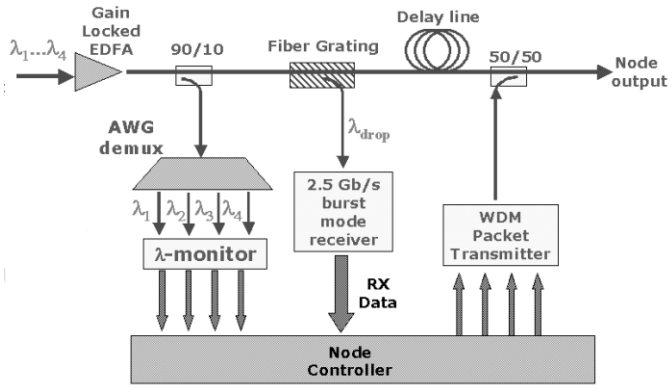

Figure 3.7: The Ringo Node Architecture [GCF+'01]

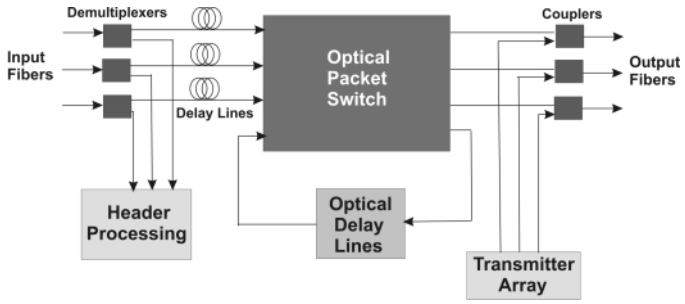

Figure 3.8: The Photonic Slot Routing Switch [ZJM'00]

Photonic Slot Routing Switch

In the photonic slot routing switch proposed by [ZJM'00] and shown in figure 3.8, channels are demultiplexed and channels containing header information are directed to the header processing unit. Corresponding data channels are delayed in fiber delay lines while the headers are processed. Then these channels are switched and eventually new data channels are generated by the transmitters and added. The architecture does not specify any provision for optical multicasting. It also does not comment on issues such as slot synchronization for dispersion compensation. It is only an overview, which does not go into technical details.

3.4 Structure of the Node and Principles of Operation

The architecture of the network proposed in chapter 2 consists of interconnected rings with nodes, which enable access to their capacity. From the previous section it can be concluded that the node architecture must functionally be similar to an OADM capable of adding and dropping packets at every node on the ring. Issues imposed on the design of the node have also been discussed in section 3.2. Based on these requirements architecture of the node is presented in figure 3.9.

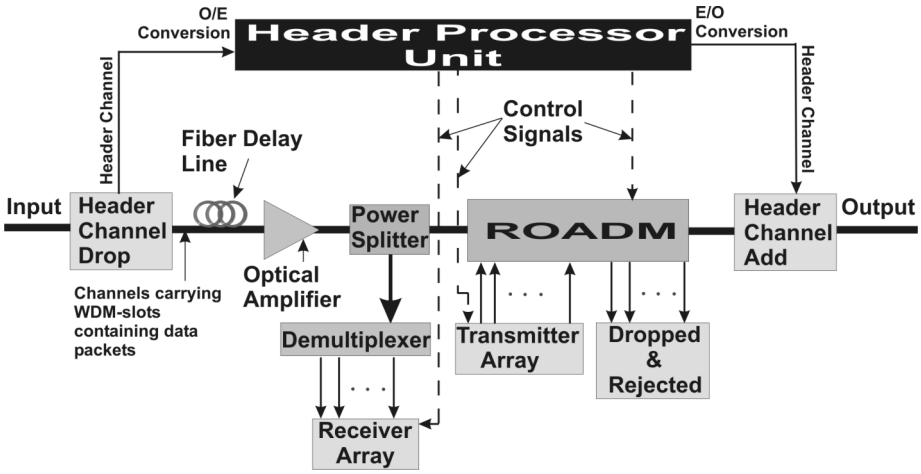

Figure 3.9: Block Schematic Diagram of the Node

The common wavelength header channel carrying slot headers is first dropped by the Header Channel Drop Unit and fed to the Header Processor Unit (HPU). The HPU receives the optical channel and processes the header in the electronic domain. The Header Channel Drop Unit allows the channels carrying WDM slots with data packets contained in them to pass through. These data channels are then delayed in a fiber delay loop while the HPU processes the slot header. The HPU, after processing the slot header, sends out three control signals, one to configure the ROADM, the second to the receiver unit and the third to the transmitter unit. The data channels meanwhile are amplified by an optical amplifier and their power is then split. Part of the power is always wavelength-demultiplexed and all data channels are received by the receiver array. The other part is allowed to pass through to the ROADM. By this time

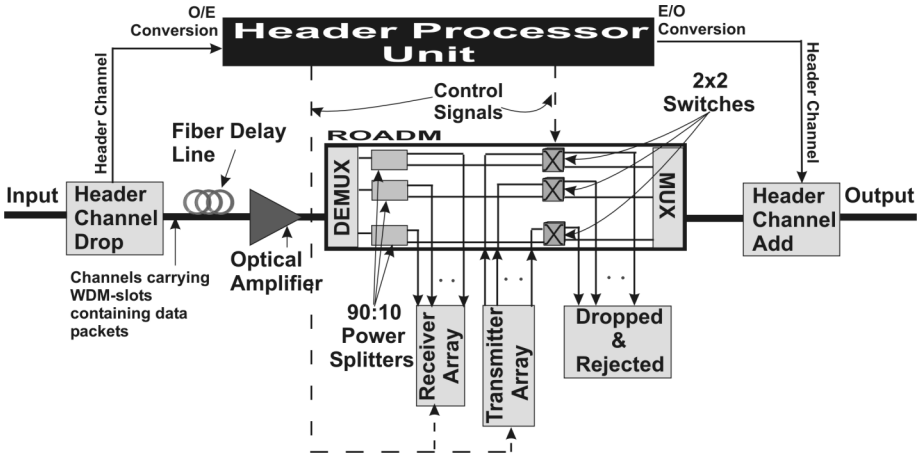

Figure 3.10: Block Schematic Diagram of the Node; Type 2

the HPU is expected to have informed the receiver array to accept or reject the received data of each wavelength channel. It is also expected to have informed the ROADM of its state and the ROADM is expected to have reached that state before the WDM slot actually arrives at it. Privacy may be a concern here, but we expect the higher layers to take care of it. The transmitter array also knows on which wavelengths it is expected to send data. At the ROADM adding and dropping takes place simultaneously. The data dropped at the ROADM is eventually rejected. In the meantime the HPU generates a new header packet and puts the header channel back into the WDM system using a header channel add unit. The central network controller conveys management information to the HPU. However, the communication between the network controller and the HPU is beyond the scope of this thesis.

Similar to the one shown in figure 3.9, the block schematic diagram of the node could also be as shown in figure 3.10. It differs from the former in that the multicasting is done using power-splitters on a per channel basis. This eliminates the need for an extra demultiplexer. However the number of power splitters grow directly with the number of wavelength channels on the ring. An alternate configuration with the usage of tri-state switches [KYZ'96] is shown in figure 3.11. The switch is set in the bar state under negative voltage, cross state under positive voltage and split state (works as a 3 dB coupler) when no voltage is applied. If the data drop section of a node is built with such a switch, the node can copy an incoming packet in optical domain permitting

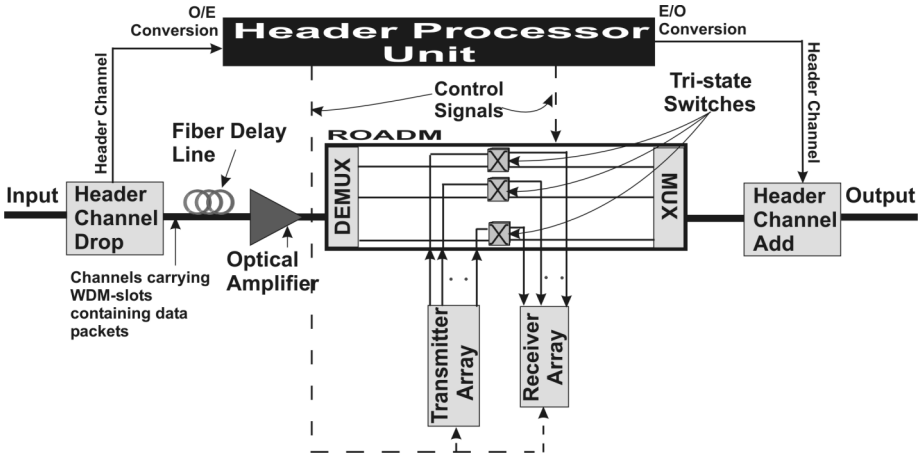

Figure 3.11: Block Schematic Diagram of the Node; Type 3

downstream nodes to access the same packet. Such operation will introduce a 3 dB power loss per traversed switch and somewhat strain the power budget of the network. Using such a technique would also result in unequal power levels of the channels. Also these switches are not commercially available and not much is known about their switching speed. Thus usage of tri-state switches is not desired. Technically there is not much of a difference between the configurations of figure 3.9 and figure 3.10. Henceforth we assume that the block schematic diagram of the node is as shown in figure 3.9.

It can be said that there are two types of delay involved in the whole operation described above: the header processing delay and the element-configuration delay. To maintain the time-gap between a WDM slot and its corresponding slot header the header processing time has to be compensated by the fiber delay line. The length of the fiber-delay line is proportional to the header processing delay. The inter-slot gap (shown in figure 2.12) can be used for changing element configurations within the node. Also it is understandable from the above description of the operating principle of the node that synchronization is needed between the dropping and the adding functions to take out a data packet and put a new data-packet exactly in its place. The sequence of events at the node is shown in figure 3.12. In the following sections the blocks making up the node and their functions are discussed in detail. With the block schematic diagram of the node presented in figure 3.9, the following sections analyze the choice of components for each block. We first discuss the most important part of the

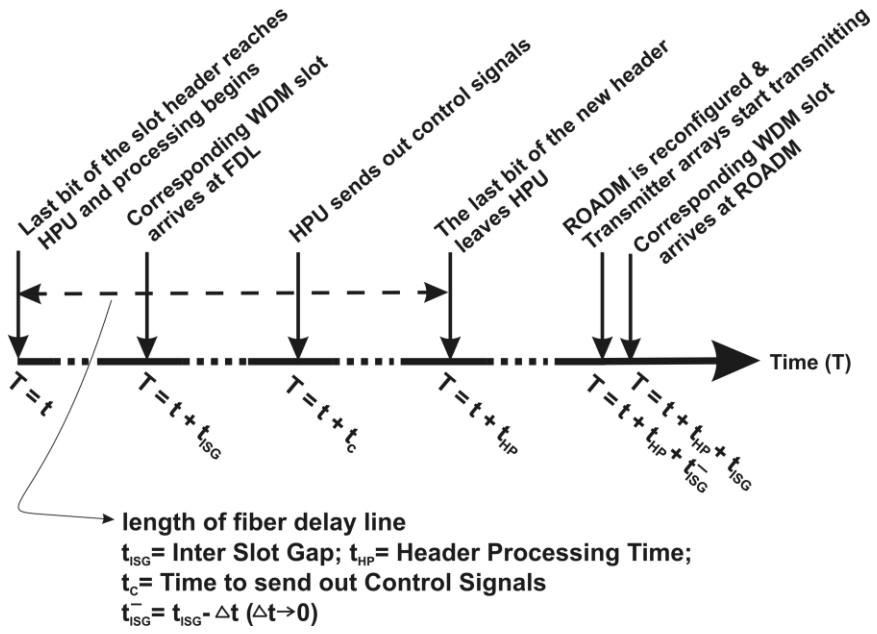

Figure 3.12: Sequence of events at the Node

node, the HPU in the following section.

3.5 The Header Processor Unit

Apart from communicating with the central network controller, the job of the HPU is to receive slot headers, process their information, carry out a few tasks based on this information and transmit a new header slot. Structurally, the HPU can generally be divided into 3 main subparts:

- optical/electrical conversion;
- processing; and,
- electrical/optical conversion;

The processing part of the HPU is functionally shown in figure 3.13. The figure shows all the necessary inputs and outputs. There may be other input and output signals based on the design of the overlying MAC protocol. But these signals are beyond the scope of this dissertation. Here only those signals are considered that affect the basic functioning of the slotted-ring network architecture of chapter 2. From the incoming signal, the processor has to recover

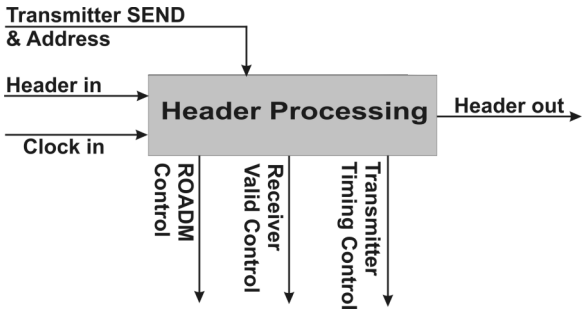

Figure 3.13: Header Processing

the packet. This is done by keeping a delimiter (a sequence of bits), which acts as a flag in the header slot to identify the arrival of a header slot. In the figure, the transmitter SEND & Address signal denotes that the node wants to send data to another node on the ring whose address is being sent via the signal. This makes the HPU aware that data packets are waiting to get access to incoming empty payload slots. The Transmitter Timing Control signal controls the exact time at which a data packet must be put onto a payload slot by a selected transmitter of the transmitter array. The Receiver Valid Control signal conveys the address of the destination node corresponding to a payload slot from the HPU to the receiver array. This is to make sure that a packet within a payload slot has not been dropped by mistake. If so it has to be stored in the electronic domain and retransmitted on the arrival of an empty payload slot at the node, where it has been dropped by mistake. The ROADM Control signal controls the operations of switches within the node to add or drop packets to or from the payload slots.

3.5.1 Clock Synchronization

From figure 2.12, it is easily noticeable that the slot headers arrive in bursts. Because of this burstiness, the clock from the slot-headers cannot be recovered using standard clock recovery techniques. For this purpose, we may use burst mode receivers, a few types of which include the following (as mentioned in [Shri'00] and [SCC'97]):

- global clock with correlator for phase detection: As shown in [EHM+'94] this technique uses a number of phase shifted versions of the local clock of the receiver. Each phase shifted clock samples the incoming data. A corre-

lation algorithm measures which phase shift has the maximum correlation with a given reference. A selector then uses this phase shifted version of the local clock to receive the remaining part of the packet. This technique uses a preamble field of a couple of bits in the packet for clock recovery. A disadvantage of this technique is that the recovered clock suffers from a phase error. Moreover, there will be a processing delay of 15 bits caused by the correlation algorithm.

- quenched narrowband tank circuit: The second technique uses a tank circuit with two different Q values as shown in [NN'90]. A low Q value during the arrival of the preamble field is used to extract the timing clock from a short preamble. A high Q value is used during the arrival of the packet data to retain the extracted clock even if less redundant codes are used. The tank circuitry is composed of a capacitor and an inductor. The resistance of a FET (Field Effect Transistor) in the tank circuitry is varied to switch the Q-value of the circuitry. The resistance of the FET is controlled by the voltage between the gate and the source. A switch controller is added to provide the signals for switching the Q-value. This technique also makes use of a short preamble field and may suffer from a frequency error, both of which will be a disadvantage.

- gated oscillators with Phased Locked Loop (PLL): The gated-oscillator technique shown in [BD'92] uses gated-oscillators to obtain a lock on the first data transition. The instantaneous locking can be done without the use of a preamble. The system contains two identical gated square-wave oscillators, whose frequency matches to a good degree (though not necessarily perfectly) to the transmission rate of the incoming signal. The oscillators are started and stopped successively by the input signal so that only one operates at any given instant of time. Their outputs are added to a NOR gate to generate the recovered clock. Each oscillator is forced into phase synchronization with the data every time it is started. Because the clock recovery is based on the transition of the input data sequence the disadvantage of this technique is that the jitter performance of the recovered clock will be the same as the input data signal. This technique also requires an local oscillator running at a frequency close to the input signal.

- Embedded Clock Transport (ECT): In this technique the transmitter

frequency-multiplexes its clock with the baseband data and modulates the optical carrier with the composite signal. This technique has been used in [Shri'00]. The technique does not require any ASICs (Application-Specific Integrated Circuit) and is therefore simple. Only a RF splitter and two filters are needed to separate the clock signal from the baseband data. Although the embedded clock technique is called a burst-mode receiver, generally speaking that is not true. Since the clock is continuously send on the sub-carrier, there is no burst to which the receiver must lock on to.

From figure 3.12 it is seen that the length of fiber delay lines at the node is equivalent to the header processing time. We assume that the slot header has a fixed size and therefore a fixed processing time and consequently the length of the fiber delay lines at all nodes are the same. The first and the second burst recovery techniques mentioned above cannot be used for they lead to unknown header processing times. The gated oscillator technique looks very promising because of its instantaneous locking. An advantage of this recovery technique is the possibility to lock the local clock a few bits after the header slot has arrived. But, the number of bits is dependent on the exact frequency alignment of the local oscillator and the incoming data signal. The ECT technique is very attractive because the clock is sent along with the header slots on a subcarrier frequency. However this technique has the disadvantage of having to deal with chromatic dispersion.

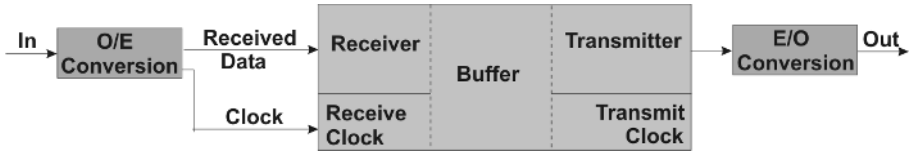

Figure 3.14: Architecture Of Master Node; type 1

Figure 3.15: Architecture Of Master Node; type 2

However, in the network proposed in chapter 2 we adopt a simple mechanism of inserting the clock signal between the header slots. Thus, the gap between the header slots is filled with the clock signal. This way, all the nodes in the ring can be synchronized with a Master node. This implies that at the Master node there will be an asynchrony between the incoming clock and the outgoing clock. There are two ways of implementing the Master node, as shown in figure 3.14 and figure 3.15. In the first case (figure 3.14), the receiver and the transmitter parts use different clocks. The receiver uses the recovered clock and the transmitter uses the local master clock. To be able to use two clocks, a buffer must be maintained to separate the two parts. In the second case (figure 3.15), the receiver and the transmitter both use the same clock. The incoming data must be phase shifted to align with a local master clock signal. The phase shift can be derived from the difference between the memory clock and the receiver clock. The first technique is easier to implement and the buffer may be implemented as a dual clock memory block.

3.5.2 The Header Processing Function

The header processing function is implemented in programmable logic. The function can be divided into two parts, the fixed hardware part and the programmable hardware part. This is shown in figure 3.13 and figure 3.16 respectively. The hardware part is the programmable chip (FPGA) with its necessary surrounding components. The programmable hardware part is the actual function of the FPGA, described in VHDL (V High Speed Integrated Circuit Hardware Description Language), which is mapped onto the logic of the FPGA.

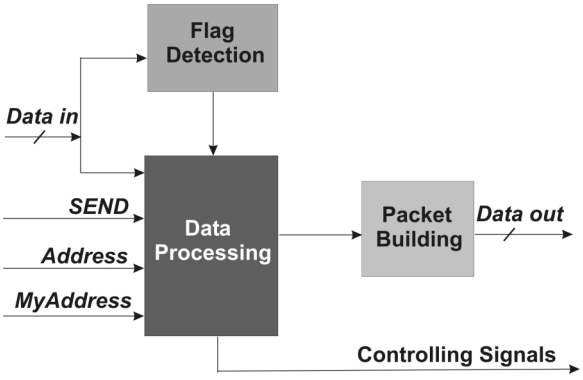

Figure 3.16: Header Processor Programmable Hardware

Hardware

The hardware consists of the programmable header processor sub-function as shown in figure 3.13. The header processor sub-function has three inputs (*Data in, Clock* and *SEND/Address/MyAddress* signals). According to the information from the *Data in* and *SEND/Address/MyAddress* signals the processor must set the Controlling Signals and generate new data for the *Data out* signal. See Table 3.2 for a description of these signals.

Signal Name	Description
Data in	Recovered data from photo detector
Send	This signal is set if the transmitter wants to send
Address	The address the transmitter wants to send to
MyAddress	The address of the current node

Table 3.2: Description of Header Processing Signals

Programmable Hardware

The functionality of the header processor is programmed in VHDL. A compiler then translates the VHDL design into a format enabling programming the hardware logic. The programmable hardware implements the following functions:

- Flag Detection: This function detects the starting and ending flag of the slot headers.
- Data Processing: When the flag is detected, this function processes the data from the slot headers. According to this retrieved data, it sets the controlling signals and makes new slot header data. The new slot header contains, apart from other information, the destination address of data packet being added onto a slot and the status (empty or full) of that slot.
- Packet Building: This function packs the new slot header data between the starting and ending flags to make a new slot header.

All the functions mentioned above are shown in figure 3.16. The data processing sub-function must set the outgoing Controlling Signals according to the received data in the slot header (*Address* and *Status*) and the *SEND* and *Address* signals from the transmitter. The outgoing Controlling Signals are *ROADM Control, Receiver Valid,* and *Transmit Timing.* The *ROADM Control* signal sets the configuration of the ROADM to the required state. This way a

Address	*Status*	*Send*	*Switch Control*	*Receiver Valid*	*Transmit Timing*	*New Data*
My/ Other	Empty/ Full	Yes/ No	Cross/ Bar	Yes/ No	Yes/ No	Old/Empty/ Addr&Full
Other	Empty	No	Bar	No	No	Old
Other	Empty	Yes	Cross	No	No	Addr&Full
Other	Full	No	Bar	No	No	Old
Other	Full	Yes	Bar	No	No	Old
My	Empty	No	Cross	Yes	No	Empty
My	Empty	Yes	Cross	Yes	Yes	Addr&Full
My	Full	No	Cross	Yes	No	Empty
My	Full	Yes	Cross	Yes	Yes	Addr&Full

Table 3.3: Header Processor Controlling Signals

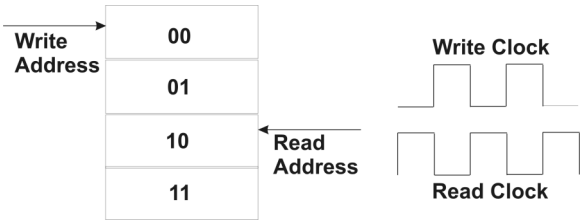

Figure 3.17: Principle Of Dual Clock Buffer

optical payload contained within the WDM slot is dropped or just sent through. The *Receiver Valid* signal tells the receiver if the received data is valid or not. It is important to note that the *ROADM Control* signal is set before the slot, which corresponds to the transmitting wavelength, is handled. Similarly, before handling the other slots, the *Receiver Valid* signal is set. The *Transmit Timing* signal is set if the transmitter is allowed to send. This signal will be sent out to the transmitter array a defined time after the slot header has been processed. This is to specify the gap between the header and WDM slot and thus adjust for chromatic dispersion effects. The data processing sub-function must also make a new slot header according to the *SEND* and *Address* signal, which are based on a data slot to be transmitted. The different output signals, which have to be set according to the input signals, are shown in table 3.3. The Buffer block in figure 3.17 acts as the buffer between the two parts of the chip running at different clocks, the received clock and the local clock. It is built up of a dual port RAM (Random Access Memory) block and 2 counters. The block solves the problem of asynchrony. It is not possible to read and write the same address

of the RAM block at the same time. So when in the worst case both clocks are completely out of phase there must be one buffer address to overcome this problem. Figure 3.17 shows the principle of the dual clock buffer. During setup, the two counters are set to 00 and 10. The counters are modulo four counters. This way the write and read address will always differ by at least one position. The receiver clock feeds the first counter and the transmitter clock feeds the second. After the buffer, all signals are synchronized with the transmitter clock.

The misalignment of slots as a result of chromatic dispersion as discussed in section 3.2.1 can be compensated for or adjusted by the transmitters' use of the *Transmit Timing Control* signal from the HPU to send data. Thus, if two slots within a WDM slot, lose their mutual alignment then on arriving at their respective destination nodes the newly added slot at this node automatically corrects the misalignment. This is shown in figure 3.18. However, for the slot that is not newly added there is no correction.

3.6 Transmitter Array

There are three major transmitter characteristics that are important in the design of multi-gigabit laser transmitters used in IM/DD systems. These include:

- **Extinction ratio**: The extinction ratio is the ratio between the average optical power for a 1-bit to the average optical power for a 0-bit. In directly modulated lasers the extinction ratio is largely determined by the modulation amplitude and the laser zero-state bias point with respect to the laser threshold. Typically extinction ratios for directly modulated DFB (Distributed Feedback) lasers range from 9 to 14 dB. A higher extinction ratio in directly modulated lasers also leads to a larger chirp. In externally modulated lasers it is determined by the modulator OFF-ON contrast. Externally modulated lasers with extinction ratios exceeding 15 dB are common nowadays. In an amplified system a poor extinction ratio will degrade system margin because the signal in the zero-state will contribute to baseband noise as a result of signal-spontaneous beat noise [Ols'89].

- **Rise/fall time and the modulated pulse shape**: A good transmitter operating at 2.5 Gbps must rise and fall to 80% and 20% of its extreme values within 150 ps. Causes of pulse degradation include electrical reflections between the laser and the driver, rise-fall time degradation due

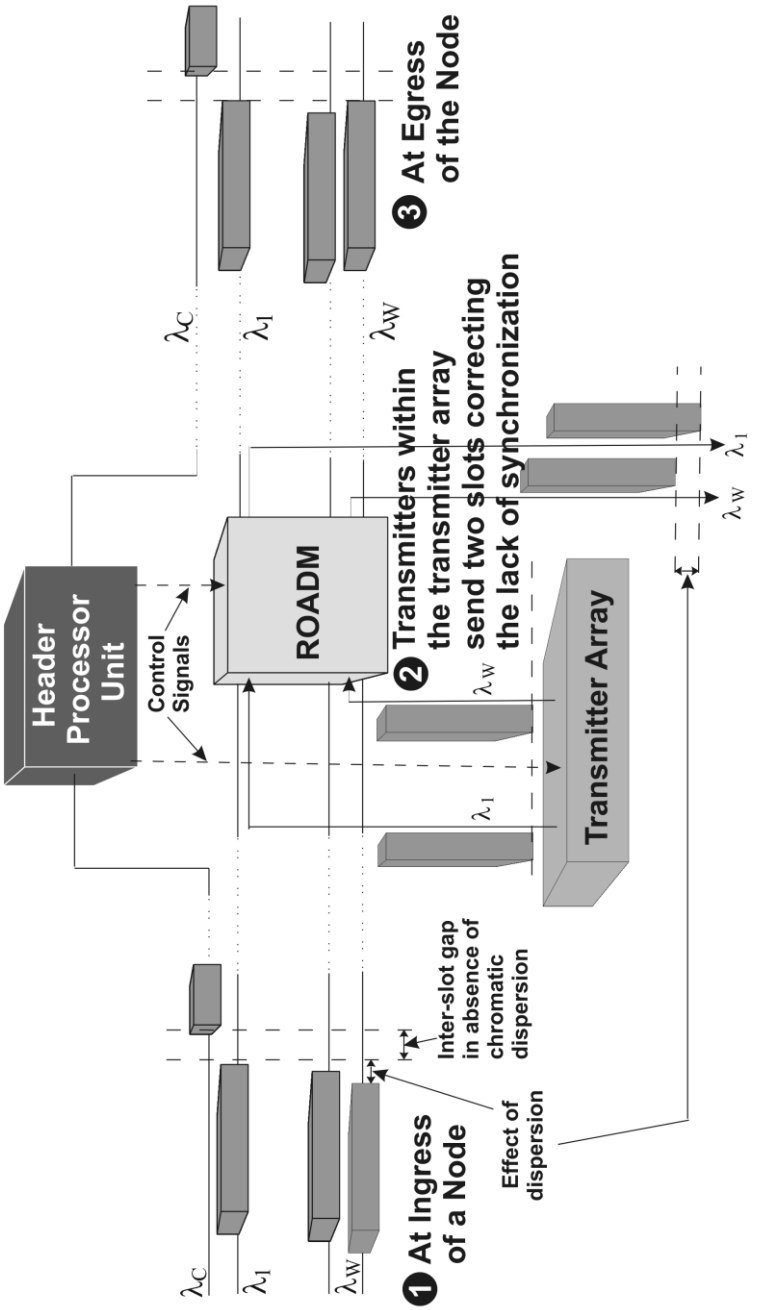

Figure 3.18: Correcting effects of Dispersion

to laser bandwidth limitations and turn-on jitter. In amplified systems, more stringent specifications are needed to provide more decision circuit eye margin for optical-SNR [Duf'84].

- **Chirping and pulse distortion**: A pulse is said to be chirped if its carrier frequency changes with time. Laser chirping will result in pulse distortions at the receiver that are proportional to the total fiber dispersion, the peak-to-peak wavelength chirp and the duration and location (leading or falling edge) of the chirp [YKW+'87]. These usually limit the transmission distance [Fis'93]. In amplified systems, together with high power levels, the presence of fiber non-linearities such as Self Phase Modulation (SPM), can alter pulses if properly designed so as to cancel chirp. This can lead to improved performance and has been discussed in [SO'93]. Directly modulated DFB lasers are known to have inherent chirp associated with the transients that constitute the information coding, although this chirp can be minimized by proper design.

Transmitters based on DFB lasers have been the choice for WDM deployments. Primary among these reasons is the excellent spectral stability, both against aging drifts and in longitudinal mode selectivity. The principal drawbacks of externally modulated lasers are the costs associated with an additional separately packaged, fiber-coupled device usually requiring polarization-maintaining fiber (leading to additional losses) and its sheer size. Concerns also remain about potential long-term drifts of the bias voltages. For the schematic of the node shown in figure 3.9, both externally modulated and directly modulated DFB lasers are suitable. However, henceforth we assume that the transmitter array comprises of an array of directly-modulated DFB lasers.

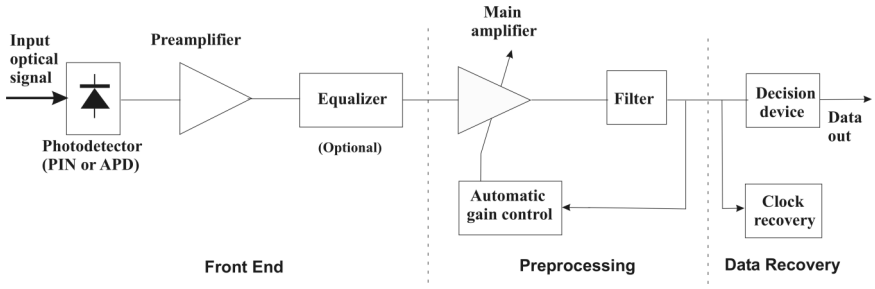

Figure 3.19: Block diagram of a direct detection optical receiver, adapted from [Mes'95]

3.7 Receiver Array

A receiver in WDM networks can be divided into three main parts: front end, preprocessing and data recovery as shown in figure 3.19. It comprises of a photodetector, an electronic preamplifier and some electronic signal processing elements. The photodetector converts the optical signal into an electrical signal with a square-law detection characteristic. Photodiodes come in two flavors: PIN [Mes'95] and APD (Avalanche Photodiode) [TMN+'96]. The amplifier provides gain and band shaping to signals from the detector. The noise added by the preamplifier should be minimized as it can affect the receiver's performance. Since there is a trade-off between noise and bandwidth, the lowest noise preamplifier designs suffer from bandwidth limitation and an equalizer is sometimes used to alleviate the problem of pulse spreading. The next step is to boost the signal with a postamplifier, usually with an automatic gain control that adjusts the gain as a function of input signal strength. The filter following the postamplifier removes unwanted frequency components. The last step is the actual data recovery. This comprises of the clock recovery circuit, which recovers the clock and feeds it to the decision device, which samples the input signal at optimum times when the signal level difference between bits '1' and bits '0' is maximum.

A PIN photodiode works on the concept of the reverse-biased p-n junction, which consists of a region known as the depletion region. When such a p-n junction is illuminated with light on one side electron-hole pairs are created through absorption. This built in electric field causes the electrons and holes within the depletion region to accelerate in opposite directions. The resulting current is proportional to the incident optical power. A simple way to increase the depletion region is to insert a layer of undoped semiconductor material between the p-n junction. Such a photodiode commonly uses InGaAs for the middle layer with InP for the surrounding n-type and p-type layers.

The idea behind the APD is to amplify the generated photo-current inside the photodetector itself before electrical amplification. This internal current gain occurs by what is known as *impact ionization* [MD'85]. The structure of an APD is similar to that a PIN except that it has an extra layer where impact ionization occurs. This layer is known as the avalanche multiplication region. However the process of impact ionization also introduces excess noise.

For the purpose of this dissertation there is not much of a difference from the architecture point-of-view in using PIN or APD receivers. However BER performance enhancement is expected with APD receivers. Also at bit rates over

2.5 Gbps it is advisable to use APD receivers because of their higher sensitivity.

3.8 Header Channel Add/Drop Module

The Header Channel Add/Drop module shown in figure 3.9 basically comprises of a tunable filter. The tunable filter helps the module switch to a spare channel as the header channel in the event of a failure in the working channel. When considering tunable filters the properties to be borne in mind include tuning range, maximum number of resolvable channels, tuning speed, attenuation, polarization independence, stability and size [Mes'95]. Most of these terms are self-explanatory. Stability implies that thermal and mechanical factors should not cause the filter transfer function to drift much. Present-day tunable filters can be broadly classified into the following categories:

- Fabry-Perot Tunable Filter (FPF)
- Mach-Zehnder Tunable Filter (MZF)
- Electro-Optic Tunable Filter (EOTF)
- Acousto-Optic Tunable Filter (AOTF)
- Semiconductor-Based Tunable Filter (SBTF)
- Fiber Brillouin Tunable Filter (FBTF)

Type	**Tuning Range** (nm)	**3 dB bandwidth** (nm)	**No. of Resolvable Channels**	**Loss (dB)**	**Tuning Speed**
Tandem FPF	50	0.01	100s	5	ms
MZI	5-10	0.01	100s	5	ms
EOTF	10	1	10	5	ns
AOTF	400	1	100s	5	μs
SBTF	1-5	0.05	10s	gain	ns
FBTF	10	$\leq$0.01	100s	gain	μs

Table 3.4: Comparison of Tunable Filters

For in-depth analysis of these filters refer to [Mes'95]. Table 3.4 summarizes their characteristics. The filters with fast tuning speeds (nanoseconds) can be

used also for packet switching. For the node architecture most of these filters are suitable. Even though packets are not switched, tuning speed is a criterion, for, the filter needs to retune to recover from a failure. Failure recovery should not take more than 50 ms as has been discussed in 2.3. Parallel to this dissertation, within the FLAMINGO project, a tunable add-drop module [RHO+'00] was being developed at the Lightwave Devices Group of the University of Twente. Figure 3.20 shows the device. The first block separates the eight wavelength channels up in odd and even numbered wavelengths. The four odd-numbered channels are sent to the next block where the ensemble is once again split up in two times two channels. This continues until one channel remains at the drop port. The remaining wavelengths are led to the combining part of the device where they are recombined in reverse order.

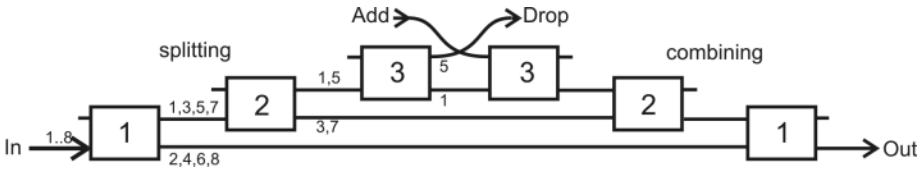

Figure 3.20: Schematic Add-Drop Multiplexer, adapted from [RHO+'00]

3.9 The ROADM

The ROADM as described in section 3.3.2 relies heavily on it switch core and its controlling electronics for performance. As shown in figure 3.6 the two main building blocks include switches and multiplexer/demultiplexer. The following section discusses key switching technologies. In section 3.9.2 multiplexer/demultiplexer technologies are analyzed.

3.9.1 Optical Switching

Although new approaches to optical switching are constantly being developed, optical switches, based on their designs, can be broadly grouped into seven main categories: optomechanical, thermo-optical, liquid crystal, micro-electrical mechanical, gel/oil based, electro-optical, SOA and ferromagnetic.

Optomechanical

In optomechanical switches electro-mechanical actuators are used to redirect a light beam. In one variety a reflective surface is inserted and retracted into a light beam to direct it between ports. In another type a grating-written fiber is bent to re-direct the light stream. Depending on the type these switches can vary in switching speed and optical insertion loss. However durability is a serious concern in these switches.

Thermo-Optical

These type of planar lightwave circuit switches are usually polymer-based or silica on silicon substrates. As the name suggests, temperature control is used to change the refractive index of the Mach-Zehnder interferometer-based waveguides on the substrate. The interaction of light in the waveguide directs it to the appropriate path and the desired port. These switches have low losses but have high driving-power characteristics and are slow.

Liquid Crystal

Liquid Crystal switches exploit the polarization states of light to allow one state to pass through the crystal in the presence of a voltage and in the absence of a voltage the orthogonal polarization state passes through it. These states are processed and recombined at the desired port to recover the original signal's properties. This technique has no moving parts, is highly reliable, but the properties of the liquid crystals are easily affected by extreme temperatures. They also have a high switching time.

MEMS

MEMS uses tiny reflective surfaces (mirrors) to redirect a beam of light to a desired port either by bouncing the light beam off other neighboring mirrors or by directly directing it to a port. The mirrors' actuators may be driven electrostatically or electromagnetically with hinges or torsion bars that bend and straighten the miniature mirrors. MEMS based switches scale easily to high port counts. The real challenge in MEMS is packaging the device itself due to the density and microscopic size of the light paths entering and exiting the substrate. MEMS-based switches are slow.

Gel/Oil Based

These switches are quite similar in operation to thermo-optical switches as the switch uses heat to operate. The difference is that heating causes a change in refractive index of air to develop at the waveguide junctions. This bubble or liquid formed redirects light through the appropriate waveguide to the desired port. This technology has proven to work with inkjet printers, albeit concerns remain about their long-term reliability, thermal management and insertion losses. They are also quite slow.

Electro-Optical

The electro-optical switch can be based on the principle of a Mach-Zehnder directional coupler switch (MZDCS), which is the following: the MZDCS is made up of two waveguides coupled at their extremities by two 3 dB couplers. In each interferometer arm, an electro-optic material introduces a phase shift. This phase shift causes destructive or constructive interference effects and enables switching in the optical domain. A wide variety of materials such as $LiNbO_3$ or InP, can be used for its implementation. The main disadvantage of some MZDCS is the large polarization sensitivity due to the polarization dependent electro-optic effect of the materials and the waveguides which are used. In addition such switches require a large driving voltage to offer a sufficiently large extinction ratio. At increasing bit rates it becomes increasingly difficult to drive these switches electronically because broadband amplifiers are needed to obtain rectangular driving signals. On the other hand it has been shown that these switches commercially exhibit high switching speeds (upto single digit nanosecond range). Typical values of such a commercial switch are: extinction ratio of 20-30 dB, insertion loss of 4-5 dB, V_{Π}(RF port) of 2.5-3.5 V and V_{Π}(DC port) of 5-6 V.

Miscellaneous Technologies

Miscellaneous switching technologies include acousto-optic, SOA and ferromagnetic based switches. Acousto-Optic switches receive acoustic-wave induced pressure from a RF-fed piezoelectric transducer to generate fine gratings in optical waveguides, which diffract light to the desired port. These switches are also slow. When injected current in a SOA is high, it passes light through with some amplification. When the injected current falls near zero, the device blocks

the light. Thus, the SOA can act as a switch. The switching time is limited by the speed at which the carrier density can be changed. For low carrier densities and square-wave control pulses, this is limited by the spontaneous lifetime of the carriers in the SOA (a few nanoseconds). Ferromagnetic technology uses magneto-optical Faraday effect that electromagnetic waves interact with each other directly to create extremely fast switches (femto seconds).

Technology	Strengths	Weaknesses	Applications
Opto-Mechanical	• Overall Performance (Insertion Loss, Crosstalk)	• Slow Speed • Scalability	• Network Protection • OADM
Thermo-Optical	• Small Size	• Slow Speed • Insertion Loss • Crosstalk, • Power Consumption, • Scalability	• Network Protection • OADM
Liquid Crystal	• Parallel Switching • Overall Performance (Insertion Loss, Crosstalk)	• Temperature Sensitivity • Slow	• Network Protection • OADM
MEMS	• Overall Performance (Insertion Loss, Crosstalk) • Scalability	• Packaging • Slow	• OXC
Bubble Switching	• Scalability	• Insertion Loss • Slow	• Network Protection • OADM
Electro-Optical	• High Speed • Reliability	• Insertion Loss • Polarization Dependence	• Network Protection • OADM • Packet-Switching
SOA	• High Speed • Loss Compensation	• Noise • Distortion	• Network Protection • OADM • Packet-Switching

Table 3.5: Comparison of Switching Technologies

Table 3.5 compares the advantages/disadvantages and applications of various switching technologies. The ones most suited for packet-switching include the SOA and the electro-optical switches. The SOA behaves as an on-off gate. It has no cross-bar functionality. A number of SOAs can be grouped together to attain cross-bar functionality. However the SOA has one major disadvantage

over $LiNbO_3$ technology. SOAs have a high noise figure which in a transparent optical network with an amplifier chain can potentially result in a low SNR at the receiver. Also $LiNbO_3$ switches are commercially very successful and easily available, making them our choice for switching inside the ROADM.

3.9.2 Multiplexer/Demultiplexer

Multiplexers/demultiplexers form the essential components of a WDM system. They enable access to each of the individual WDM channels. Multiplexers in use today can be primarily classified into four categories: AWG, dielectric thin film filters (DTFF), diffraction gratings (DG) and fiber Bragg gratings (FBG).

Arrayed Waveguide Gratings

An AWG device, sometimes called an optical waveguide router or waveguide grating router, consists of an array of curved-channel waveguides with a fixed difference in the path length between adjacent channels [ABH+'94]. The waveguides are connected to cavities (open regions without waveguides) at the input and output. When light enters the input cavity, it is diffracted and enters the waveguide array. There the optical length difference of each waveguide introduces phase delays in the output cavity, where an array of fibers is coupled. The process results in different wavelengths having maximal interference at different locations, which correspond to the output ports. One major disadvantage of AWGs is that they are very temperature sensitive (sometimes compensated by thermo-optic polymers).

Dielectric Thin Film Filters

The structure of a thin-film filter is based on that of the Fabry-Perot (F-P) etalon, which is composed of a cavity and mirrors and which acts as a bandpass filter [SS'96]. The center wavelength of the passband is determined by the cavity length. They exhibit a very low polarization dependence when used at near normal beam incidence.A narrow thin-film interference filter for WDM consists of more than two F-P cavities separated by dielectric reflection layers, and each cavity contains a multilayer structure with more than 50 layers. The two kinds of layers are deposited alternately on a glass substrate with a unit thickness of half the target wavelength, and the materials used for the layers are usually SiO_2 and TiO_2 because of the large difference between their refractive indices. The

passband shape of a WDM filter improves as the number of cavities increases. It has thus become possible to obtain filters with a loss of less than 0.5 dB, a wide band, and a low crosstalk. A WDM multi/demultiplexer can be formed by cascading thin-film filters with different wavelengths in series. However, it is rather difficult to reduce the wavelength spacing and increase the port count of this type of multi/demultiplexer because making a thin-film filter with a narrow passband becomes more difficult, the assembly cost increases, and the insertion loss accumulates at each stage.

Diffraction Grating

Grating based demultiplexers use the phenomenon of Bragg diffraction from an optical grating [NR'92]. A reflection grating splits the input WDM signal incident on it into various components spatially and a lens focuses them onto individual output fibers. The focusing lens can be eliminated altogether by the use of a concave grating.

Fiber Bragg Grating

A fiber Bragg grating is made from a section of ordinary single-mode optical fiber, typically a few millimeters to a few centimeters in length. The grating is formed by causing periodic variations in the index of refraction of the glass lengthwise along the fiber [AR'94]. The period of the index modulation can be designed to cause deflection of light at a specific wavelength, the Bragg wavelength. Typically the light at the Bragg wavelength is selectively reflected while all other wavelengths are transmitted, essentially unperturbed by the presence of the grating. By combining fiber gratings in various arrangements, many different wavelengths can be separated and coupled out. A fiber Bragg grating's low-loss characteristics and its ability to selectively pass or reflect specific frequencies, make it a very versatile element that can be used in filters and de-multiplexers for wavelength division multiplexing networks.

The above technologies differ from each other in their characteristics: the passband of one may be flatter than the other; a channel in one may have more crosstalk with its adjacent channel than in the other; and one may have a higher insertion loss as compared to the other. Today demultiplexers based on thin film filters are increasingly gaining importance because of their stable characteristics (with respect to temperature and mechanical stress), their low insertion loss and a low adjacent channel crosstalk of less than -35 dB. For the purpose of this

dissertation all the technologies mentioned above are equally suitable. However for the sake of conformity, in the remainder of this dissertation, when referring to demultiplexers dielectric thin film filters are implied. Cascading of filters leads to passband narrowing. Usage of passband-flattened filters minimize this but do not completely eliminate the problem of passband narrowing.

3.10 Optical Amplifier

Two major types of optical amplifiers are in use today. These include fiber amplifiers and SOAs. Other types of optical amplifiers include Raman ([ZLS+'01]) and Brillouin ([JSS'95]) amplifiers and Praseodymium amplifiers ([SDP+'96]).

The doped fiber amplifier is a length of fiber doped with rare-earth metal ions, such as erbium, Er^{3+}. The ions create an active medium. Carrier inversion occurs in the presence of a pump leading to spontaneous emission. The pump is chosen such that its wavelength is preferentially absorbed by the ions. In the presence of an optical signal stimulated emission occurs leading to amplification. EDFAs ([MRJ+'87], [DSB'87], [Des'94]) have played a major role in the commercialization of WDM networks, because of the EDFAs ability to amplify many channels simultaneously in he 1530–1560 nm window.

SOAs ([O'Ma'88], [SM'87], [Fye'84]) are basically semiconductor lasers with or without facet reflections. An electrical current inverts the medium by transferring electrons from the valence band to the conduction band. This inversion causes spontaneous emission. The presence of an optical signal leads to stimulated emission thus yielding signal gain.

The key performance parameters of optical amplifiers are gain, gain flatness, noise level, polarization dependence and output power. Gain should be flat because all the WDM signals must be equally amplified. The gain profile of EDFAs is wavelength-dependent although it can be corrected with gain-flattening filters. Noise is extremely crucial in optical amplifier chains. SNR is probably the biggest limiting factor in cascading amplifiers thereby decreasing reach.

The performance of both SOAs and EDFAs are affected by the spontaneous emission noise. Table 3.6 compares the two types of amplifiers. When compared to EDFAs, SOAs have two major drawbacks: firstly, the carrier lifetime in SOAs is far smaller than that of EDFAs. This leads to interchannel crosstalk in the presence of more than one intensity modulated signal in an SOA; and, secondly, SOAs have a higher noise figure as compared to EDFAs. An EDFA (with

multiple pump lasers) is more reliable than an SOA. As a result EDFAs have been widely used as a WDM amplifier. In view of these advantages, EDFAs are preferred to SOAs as optical amplifiers in the node architecture of this dissertation.

Type	Pumping Source	Life-time	Insertion Losses	Operating Wavelength	Gain	Noise Figure
SOA	Electrical (100 mA)	1 ns	3 dB	1.3 or 1.5 μm	10-15 dB	8-12 dB
EDFA	Optical (20-50 mW)	1 ms	0.2 dB	1.55 μm	10-40 dB	4-5 dB

Table 3.6: Comparison of SOAs and EDFAs

3.11 Power Budget Calculations and Splitting Ratio

The sections above describe and motivate the technology of choice of each network element shown in figure 3.9. With the insertion losses of these devices at hand it is worthwhile to make a power budget calculation and thereby decide upon the splitting ratio of the power splitter in figure 3.9.

Device	Insertion Loss
SMF at 1550 nm	0.22 dB/km
Thin Film Filter Mux/Demux (incl. ROADM)	4 dB
Electro-Optic Switches (incl. ROADM)	4.5 dB
Header Channel Add/Drop Module	5 dB

Table 3.7: Insertion Losses

Sensitivity of an APD receiver at a BER of 10^{-12} (using a pseudo random $2^{23}-1$ bit sequence) at 2.5 Gbps at a wavelength of 1550 nm is roughly -34 dBm. For a more detailed analysis of the sensitivity of receivers refer to [RS'98]. We assume that the average power emitted by a 2.5 Gbps transmitter is 2 mW (3

dBm) and that the number of WDM channels equals four, including one channel reserved for carrying slot headers. Assuming the device losses shown in table 3.7 and that the nodes are separated by a distance of maximum 20 kilometers of standard SMF, we get at the input of the optical amplifier in figure 3.9 a power of approximately -20 dBm per channel. Using an EDFA as an optical amplifier and assuming that the gain per channel of the EDFA is 27 dB (that is operating the EDFA close to the small-signal gain region) we obtain at the input of the power splitter roughly 7 dBm per channel. It is therefore enough to use a 90:10 splitter and drop only 10% of the power. Doing so, leaves the receiver with approximately -7 dBm and thus the receiver has enough margin (assuming 8-10 dB as system margin) for power penalty from crosstalk and other signal degradations. The power that passes through to the ROADM is roughly 6.5 dBm. It undergoes a 4 dB loss at the demultiplexer within the ROADM and at the ingress of the switch has a power of roughly 2.5 dBm. Table 3.8 shows the accumulation of optical power loss at the node. Thus at the switches channels coming from upstream nodes have approximately the same power level as those newly generated by the transmitter arrays. It is always desirable to keep all the channels within a WDM system at equal power levels for reasons described in section 3.2.2. The link lengths in practice are assumed to vary between 10 and 20 kilometres. This implies that the link losses could vary between 2 and 4 dB. Losses arising from other devices are assumed to be constant.

Device	**Input Power**	**Output Power**
Transmitter		3 dBm
Switch	3 dBm	-1.5 dBm
Multiplexer	-1.5 dBm	-4.5 dBm
Fiber	-10.5 dBm	-14.5 dBm
Header Channel Drop Module	-14.5 dBm	-19.5 dBm
EDFA	-19.5 dBm	7 dBm
Power Splitter	7 dBm	P_1 = -3 dBm P_2 = 6.5 dBm
Demux in front of receiver	-3 dBm	-7 dBm
Receiver	-7 dBm	
Demux within ROADM	6.5 dBm	2.5 dBm

Table 3.8: Accumulation of optical power loss in the node (according to figure 3.21)

3.12 The Complete Node Architecture

The structure of the node and its principles of operation have been described in 3.4. In that section the basic modules and their functions were also proposed. In subsequent sections, technologies for these modules were analyzed and some technologies were found to be more suitable than the others. Incorporating components based on these preferred technologies for these modules the complete architecture of the node is depicted in figure 3.21, which will be referred to as the node architecture in the remainder of this dissertation.

3.13 Conclusions

In this chapter the node architecture was gradually built-up by first identifying and analyzing the system issues enforced by the network architecture of chapter 2 and others that go hand-in-hand with optical fiber networks in general. Types of node architectures prevalent in today's WDM network were discussed in section 3.3. Consequently a block schematic diagram of the node was proposed in section 3.4. Using this as the reference, technologies for each of the blocks were analyzed and preferences were presented. Finally, a power budget calculation was made in section 3.11 and the complete node architecture depicted in figure 3.21.

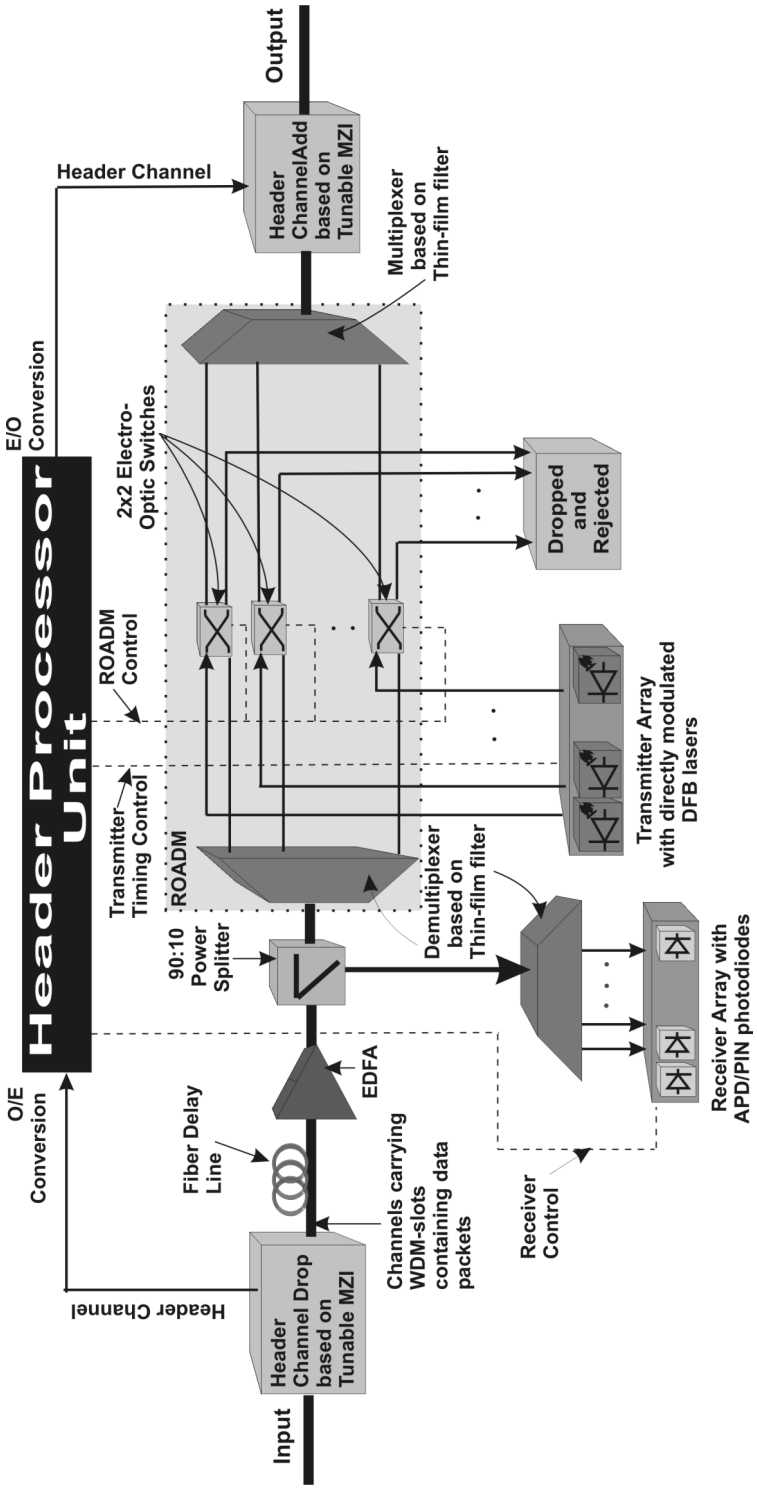

Figure 3.21: Architecture of the Node and its Components

CHAPTER 4

Performance of the Network and the Node

4.1 Introduction

Simulation techniques can be resorted to as a first hand approach towards understanding the functioning of the FLAMINGO network, its node and the header processing functions. The simulation activities involving the network and node architectures presented in chapters 2 and 3 can be broadly classified into 2 parts:

1. Simulation of the Header Processor Unit (HPU) to aid in its implementation. For this purpose it has been assumed that slots travel unidirectionally in a ring with three nodes and two data channels. The header comprises of two 16-bit delimiters enclosing two 4-bit packets. Of these 4 bits, 3 bits are used to address a node on the ring and 1 bit to describe the status of a slot within a corresponding WDM slot.

2. Simulation of the optical part of the network and the node to have a general overview of its performance. We have used for this purpose simulation software, *VPITransmissionMaker* and *VPIComponentMaker* under license from Virtual Photonics Incorporated (VPI).

Part one is necessary to ultimately realize the HPU in the laboratory. We intend to run the HPU at 155 Mbps with an option to scale it up to 622 Mbps. The motive of part one is to demonstrate that the header processing functions are indeed possible in the electronic domain. Part two deals with crosstalk effects and SNR degradation of optical signals as they pass through nodes (figure 3.21) in the network proposed in figure 2.19, and is needed for the overall network design.

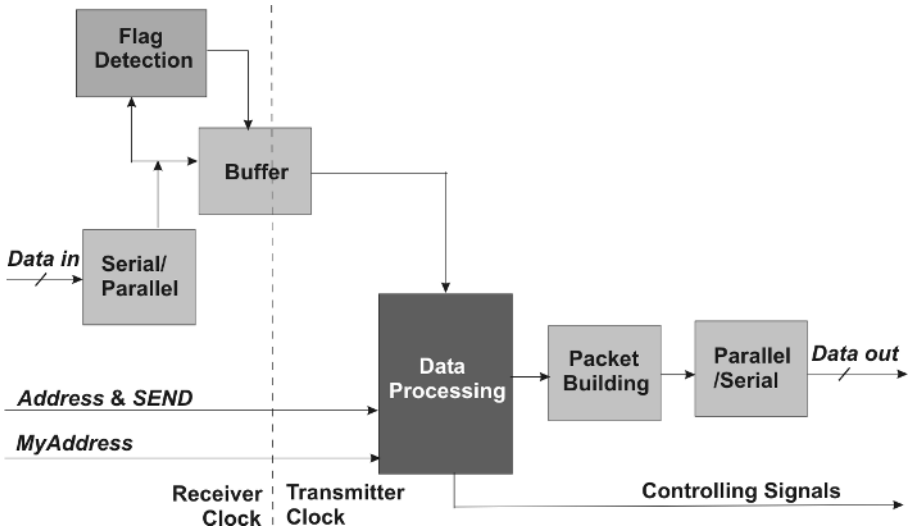

Figure 4.1: Block Schematic for the Programmable Hardware

4.2 The Header Processor Unit

Now that the architecture of the header processor unit is known (section 3.5), we proceed with the first part of the implementation, the design of the programmable hardware. The functions to be implemented in this hardware are shown in figure 4.1.

4.2.1 VHDL description

Programmable hardware can be described at different levels. One of the more abstract ways of describing programmable hardware is to use VHDL (VHSIC Hardware Description Language, VHSIC means Very High Speed Integrated Circuit). This is a language which can describe the hardware in an abstract

fashion (but also a detailed description in terms of AND-ports and flip-flops is possible). The purpose of using such an abstract language is to implement certain functions in the chip without knowing much of the underlying hardware technology. The VHDL code can be translated towards hardware by a synthesizer. Usually the synthesizer used for a certain chip comes from its manufacturer. The synthesizer translates the VHDL code into the functions available in the FPGA. The synthesizer also tries to place and route (interconnect) these functions in such a way that the given timing or area requirements are met. Another advantage of VHDL is that it allows the making of test benches. The test benches are also described in VHDL. This way a code can be checked independent of the type of the simulator. To produce waveform outputs a specific simulator is necessary. The waveform file will therefore not be independent of the simulator used.

For the design of the header processor, the different functions from figure 4.1 were first described in VHDL. This is done with the program **Modelsim**. This program has a VHDL editor and can do a functional simulation of the VHDL code and produces waveform outputs. Every function block in figure 4.1 is implemented in a VHDL file. The different interfacing signals determine the inputs and outputs of the VHDL files. A master file is used to connect all the different functional blocks. When the VHDL code functions as wanted, it can be translated into hardware.

4.2.2 Choice of Processor

The selection of the chip to be deployed starts by assuming that an FPGA (Field Programmable Gate Array) will be used. Designing and programming such a FPGA and an accompanying PCB (Printed Circuit Board) requires specific knowledge, which makes Xilinx and Altera FPGAs preferable. There are three major criteria on which the choice is based:

1. Since the programmable hardware has to run at 155 Mbps the chip used must be able to handle this speed.

2. The chip must support LVDS (Low Voltage Differential Signal) or PECL I/O.

3. There must be some designing knowledge of the chip available with the laboratory personnel.

Firstly, if the chip cannot handle the line speeds, the function can never be implemented. An option can be made to see if a chip will support higher line speeds. This can be convenient for future designs. The second item is a constraint that follows from the optical receiver module and laser module to be used. These modules are assumed to have differential PECL outputs or inputs (based on the existing components in our laboratory). It will be very useful for the FPGA to have a differential I/O support. This way no translations have to be done. These translations cause extra delay in the system. Furthermore the differential lines can handle much higher speeds since they are less sensitive to environmental influences.

Given the criteria above, the choice is made for the Altera 20KE family. The larger members of the 20KE family support LVDS at 155 Mbps and at even higher speeds. There is a lot of designing experience of the Altera chip available with the laboratory personnel. Also, all the software necessary for the design is already present. Furthermore the chip provides scalability to handle larger header packets at higher line speeds of upto 800 MHz.

4.2.3 Programmable Hardware Design

The VHDL files made were mapped onto the Altera device using the **Quartus** tool. This is the program from Altera which supports the 20KE family and can map VHDL files onto the programmable hardware. But the program could not directly map the VHDL files, made in **Modelsim**, onto the device given the required speed (155 MHz). The most likely reason for this is that the self-made VHDL code was not optimized for the Altera chips. So another way of designing the programmable hardware had to be used. In the **Quartus** tool Altera has defined some macro functions. These are VHDL, AHDL or Verilog code for a specific function. Since the code in these macro functions is optimized for the Altera chips the synthesizer is able to map these macro functions onto the chip with the given timing constrains. A disadvantage of doing this is that some of the abstraction is lost and also other processors from other manufacturers can no longer be used with the same VHDL code.

Figure 4.2 shows the design in an simplified block schematic. The figure sums up the functions from figure 4.1 as given in the **Quartus** design. The different functions are given together with their name in the design and the unique instant number (inst). Also the names of the input, output and internal signals are stated. Except for DATAPROC, SERIALIZER, DCBUFFER and

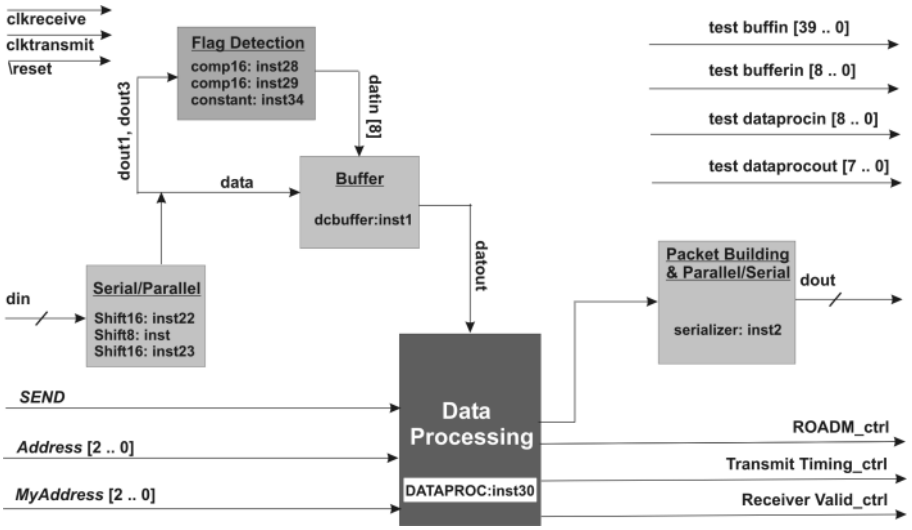

Figure 4.2: Simplified Block Schematic of the Quartus Design

DELAY all the blocks are Altera macro functions. The DATAPROC block still contains self made VHDL code. The SERIALIZER block, DCBUFFER block and DELAY block are hierarchical blocks containing block schematics of their own. All the blocks will be described in the following section.

Description of the Quartus Design

Here a description is given of the design of the header processing function made with the **Quartus** tool. The description refers to the schematics from figure 4.2. The functions of all blocks and the signals, which interconnect them with other blocks are described. The blocks are uniquely marked by their so called instance number (inst).

The blocks Shift16 and Shift8 (inst, inst22 and inst23) form the deserializing shift register (40 bits wide). The first 16 bits and the last 16 bits (signals *dout1* and *dout3*) are compared to a constant value representing the flag (1111000011110000 in binary equals 61680 in decimal). This is done in the comp16 blocks (inst28 and inst29). When the flags are detected the comparator gives a valid signal (signal *datin[8]*). This signal is sent together with the intermediate 8 bits from the shift register representing the header data into the DCbuffer block. This block (inst1) is the buffer between the two parts of the chip running at different clocks. The valid signal also resets the incoming shift

register blocks. This is done to ensure the second flag of a packet is not twice detected as the first flag of a following packet.

The DC buffer block is built up of a dual port RAM block and two counters (resp. inst 2 and inst 1 and 3, see figure C.1 of Appendix C). The RAM block is 9 bits wide (eight data bits and the valid bit) and four words deep. This block has to solve the problem of the asynchrony. Therefore the buffer has to be four words deep. It is not allowed to write and read the same address of the RAM block. So when in the worst case both clocks are completely out of phase there must be one buffer address to overcome this problem. The principle of the dual clock buffer has been shown in figure 3.17. During setup the two counters are set to 00 and 10 respectively. The counters are modulo four counters. This way the write and read address will always differ two positions. The first counter is fed by the receiver clock, the second counter is fed by the transmitter clock. After the buffer all signals are synchronized with the transmitter clock. The signals are fed in the DATAPROC block together with the SEND, Address and MyAddress signals. Based on these input signals the DATAPROC block (inst 30) determines the new header data, a valid bit and the controlling signals. See Appendix A for the VHDL code of the DATAPROC block. The outputs of the DATAPROC block are calculated from the input signals according to table 3.2 from section 3.5.2. The controlling signals are led directly to the output of the device.

The new header bits derived in the DATAPROC block are led to the hierarchical block SERIALIZER (inst2). See figure C.2 of Appendix C for the design. This block packs the new header data between two flags and sends the generated header packet serially out. When the valid bit is true the 40 bit shift register (inst, inst3 and inst4) is loaded with the flags and the new header data. The valid bit also sets the CNTR block. This block enables the shift register to shift its data out for 40 clock pulses. This is a self made VHDL block (see Appendix A for the code). In the BUSMUX block the valid signal from CNTR sets the signal from the shift register to the output. At any other time the signal from the TOGGL block is led to the output. The TOGGL block is a self made VHDL block which generates the clock signal used in between two consecutive header packets (see Appendix A for the VHDL code).

Extra test signals are given to the output to be able to monitor signals inside the chip once it is programmed and runs in the system. Table 4.1 shows the names of the test signals and their function. Also shown in figure 4.2 are some global input signals. These are *clkreceive*, *clktransmit* and */reset*. These

are respectively the recovered clock for the receiving part, the local clock for the transmitter part and a global reset signal which can reset all the internal registers.

Name	Function
test_buffin[39..0]	outputs of the input shift register
test_bufferin[8..0]	input of the DCBuffer block
test_dataprocin[8..0]	input of the DATAPROC block
test_dataprocout[7..0]	output of the DATAPROC block

Table 4.1: Test Signal names

4.2.4 Design Results

The results of the programmable hardware implementation can be split up into two parts. The functional part checks whether the design functions as desired. The timing part predicts the timing parameters of implementation. These timing parameters are important to predict if the design works correctly once implemented.

Functional tests

For the functional simulation two actions were taken. The first one is to make a test bench for the VHDL code of the data processing block. This block is an important block since it sets the controlling signals according to the received data and builds the new header data. By building a test bench in VHDL the code can be functionally checked when simulated. The test bench is shown in Appendix B. By giving several input vectors and the accompanying outputs the simulator will give an error if the calculated outputs are different. In table 4.2 a couple of test vectors used in the test bench are shown. According to these test vectors the VDHL code for the data processing block can be stated as correct.

The functional simulation of the total design made in **Quartus** can only be checked by the use of the simulator. See figure 4.3 for the simulator waveform. The waveform shows the incoming header packet on *din*. It shows the flags (1111000011110000) and the data in between (01011001); the other input signals are *SEND*, */reset*, *myaddress*. These signals are all based on the first data row from table 4.2. Also the two clocks are shown. The *clkreceive* channel is the receiving clock at 155 MHz. The *clktransmit* is the transmitting clock at 19.44 MHz. This clock is internally boosted to 155 MHz. This is done because it is

Data in	addr in	my addr	valid in	SEND	reset	data out	A	B	C	valid out	function
00000000	100	010	0	0	1	00000000	0	0	0	0	reset vector
00000000	100	010	0	0	0	00000000	0	0	0	0	reset
00000000	100	010	0	0	0	00000000	0	0	0	0	reset
01011001	100	010	1	1	0	10011001	1	1	0	1	first data
01011101	100	010	1	0	0	00001101	1	0	0	1	data
01010101	100	010	1	0	0	00000000	1	0	1	1	data
01010101	100	010	1	0	0	00000000	1	0	1	1	data
01010101	001	010	1	1	0	00110000	1	1	1	1	data
01010101	001	010	0	1	0	00000000	0	0	0	0	data

Table 4.2: Test vectors test bench; A = ROADM state; B = Transmitter Timing; C = Receiver Valid

more easy to make an 19.44 Mhz crystal oscillator to generate the local clock. The boosted signal is also shown (*altclklock*). The output signals are also shown and are according to table 4.2.

Timing tests

After the functional tests are completed the timing can be investigated. There are two timing simulations that are important. The first one is the timing parameters calculated by the synthesizer. The synthesizer estimates these timing parameters dependent on the placing and routing being done. The synthesizer assumes the worst case parameters. So the specifications coming from this simulation are worst case specifications. The second timing simulation involves the waveform simulator again. In this simulation, the simulator takes the timing as well as the function into account and presents it as a waveform file. This file is important to see how much delay is introduced by the header processor. The timing parameters calculated from the synthesizer are show in table 4.3.

Timing	Signal	Value
Shortest slack time	clkreceive	1.042ns
Shortest slack time	clktransmit	1.401ns
Setup time	din	3.730ns
Hold time	all inputs	$\leq$0ns
Clock to Output time	dout	5.702ns

Table 4.3: Timing parameter

The most important parameters are the slack times for the two clocks. The

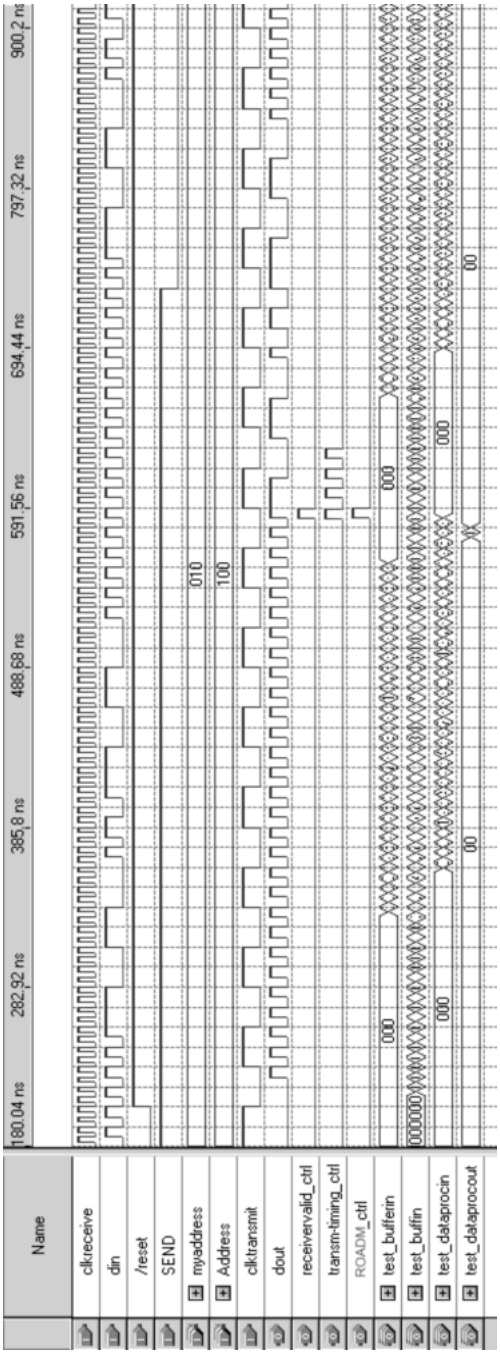

Figure 4.3: Waveform1

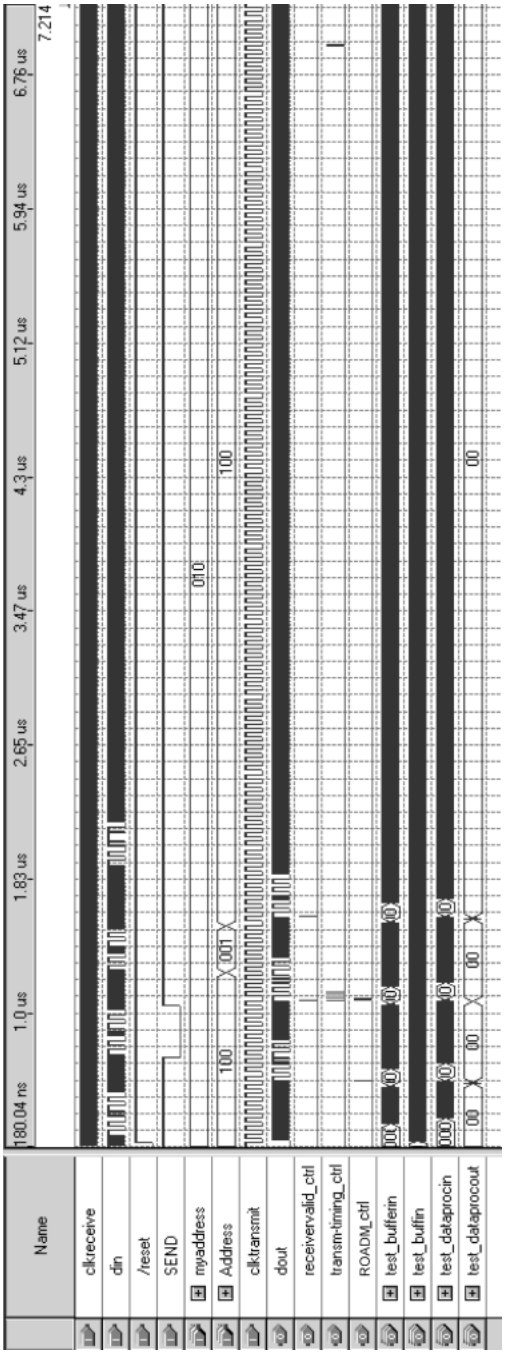

Figure 4.4: Waveform2

slack time is the margin by which a timing requirement was met or was not met. A positive slack indicates the requirement is met. The slack times follow from the required frequency, *fmax*, which in this case is 155 MHz. Since the implementation of the chip has complex timing assignments the slack time is calculated for each clock instead of the maximal achievable frequency. The other values from table 4.3 indicate the parameters which the input and output signals meet. The hold time is zero because of the use of the clock-lock function. This function transports the clock evenly over the chip in such a way that the hold time can be zero. This results in a small increase in the setup time.

The output of the timing simulation in the waveform simulator is shown in figure 4.3. The figure shows a header processing delay of 327.24 ns. This delay is induced by two parts. The main part is getting the 40 bits of the slot header in. This takes most of the time (40 bits * 6.43 ns/bit = 257.2 ns). The delay induced by the processing itself is 11 clock cycles ($11 * 6.43 = 70.73$ ns) because the path from *din* to *dout* contains 11 registers. This is observed in figure C.3 of Appendix C. Figure 4.4 shows the output of the timing simulation in the waveform simulator on a bigger time scale.

4.3 Simulating the Performance of the Physical Layer

This section presents the performance of the network and the node. The simulation setup is presented in 4.3.1. Subsequently, the results of the simulation are presented in 4.3.2.

4.3.1 Simulation Setup of the Physical Layer

For simulating the physical layer, VPI (Virtual Photonics Inc.) simulation software was used. The network was simulated as a single 4 wavelength WDM bidirectional counter-rotating ring with adjacent nodes separated by 20 kilometers of standard singlemode fiber. Each wavelength was modulated with a $2^7 - 1$ PRBS data stream at 2.5 Gbps. The WDM system was centered around 193.1 THz (1552.52 nm) with a channel spacing of 100 GHz. Most of the modules used in the simulation and their parameters are discussed next.

The transmitter modules comprise of directly modulated DFB lasers. Under NRZ modulation the lasers had a mean power of 3 dBm and an extinction ratio

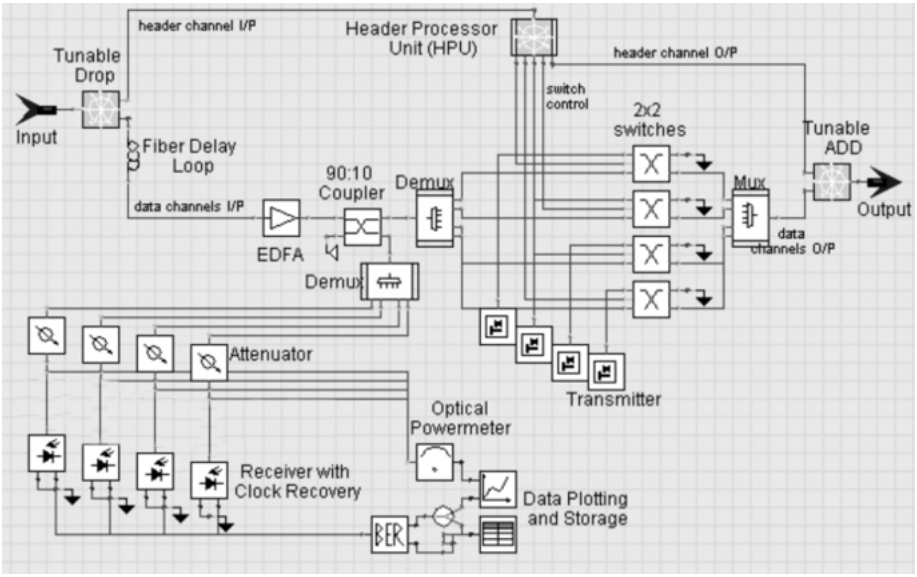

Figure 4.5: Simulated Node Architecture in VPI

of 12.5 dB. Their side mode suppression ratio was 30 dB with a side mode separation of 80 GHz. They had a linewidth of 10 MHz. The rise and fall times of the transmitters were 130 ps and 150 ps respectively. The lasers had an emission frequency drift of 1.0 GHz/K with a maximum allowable temperature drift of 4 K from the reference temperature of 25°C. At a power of 3 mW the Relative Intensity Noise (RIN) was -130 dB/Hz.

The WDM Multiplexer/Demultiplexer modules are comprised of optical bandpass filters to provide an adjacent channel isolation of at least 25 dB and non-adjacent channel isolation of at least 40 dB. The 3 dB bandwidth of the filters was set at 40 GHz.

The optical switch module comprises of a 2x2 electro-optic $LiNbO_3$ switch. The crosstalk between the input signals was on an average 25 dB.

The EDFAs had a small-signal gain of 26 dB and a maximum signal output power (excluding Amplifier Spontaneous Emission) of 20 dBm. They were assumed to have a noise figure of 5.0 dB.

The receiver modules comprise of a PIN photodiode. The noise is assumed to have Gaussian statistics and the total noise is given by the sum of the statistical independent noise sources of the signal-ASE beat-, ASE-ASE beat-, thermal- and shot noise and dark current. The thermal noise was set at 10 pA/$\sqrt{}$Hz.

Dark current was set at 10 nA. The photodiode had a bandwidth of 30 GHz and a responsivity of 0.8 A/W. The optical amplifier had an unsaturated gain of 10 dB with a saturation output power of 10 mW. The noise figure was set at 5.0 dB.

All fibers are assumed to be standard single-mode. Figure 4.5 shows the simulation model circuit of the node in VPI.

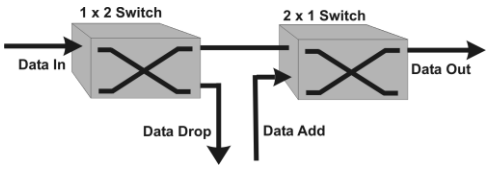

Figure 4.6: Dilated Switch

4.3.2 Simulation Results

The simulation setup was varied to have an estimate of (1) the change in the BER for an increase in the number of intermediate transparent nodes as seen by a channel from its source node to its destination node and (2) the effect of in-band crosstalk on the BER degradation. For the former those connections were compared, whose distance between source and destination vary by one node. To observe the effect of accumulating in-band crosstalk a comparison was made between three situations: first, in which a slot was to be refilled with a data packet at its destination (that is spatial reuse); second, in which a slot was to be refilled at the node downstream to the destination node (restricted spatial reuse) and third, by the usage of dilated switches in combination with spatial reuse (thus refilling the slot at its destination). The impact of dilated switches on inband crosstalk has also been studied by [Vee'99]. Figure 4.6 shows the architecture of a dilated switch. At the nodes the inband crosstalk arises primarily at the 2x2 $LiNbO_3$ switches due to improper isolation of the undesired channel. This undesired channel is at the same nominal wavelength as the desired one. However, they originate at different sources and thus are not phase correlated.

Figure 4.7 shows the effect of an increase in the number of transparent nodes on the BER with spatial reuse and using 2x2 $LiNbO_3$ switches. From the figure it can be observed that at a BER of 10^{-14} and a received power greater than -20 dBm it is possible to support up to 8 nodes on a bidirectional ring (implying up

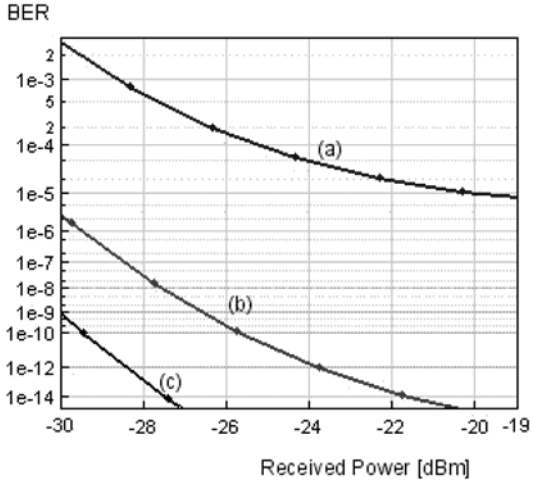

Figure 4.7: Graph showing the effect of increasing number of transparent nodes: (a) 10 transparent nodes, (b) 8 transparent nodes, and, (c) 6 transparent nodes on a single bidirectional all-optical ring

to 3 intermediate transparent nodes for any connection between its source and its destination nodes). The BER degradation gives rise to a BER floor when 10 nodes are present on the ring. This implies that if the BER floor is fixed there exists an upper bound on the number of nodes that a single ring can potentially support [DKB'02].

Plots (a) and (b) of figure 4.8 indicate the change in BER when the slot is reused at the destination node and when the slot is reused at a node downstream to the destination node. From the plots we observe that the former case leads to a power penalty of approximately 2 dB at a BER of 10^{-9}. Plot (c) indicates the change in BER when using dilated switches. The insertion loss of a dilated switch was assumed to be twice that of a single 2x2 $LiNbO_3$ switch and the crosstalk between input signals was assumed to be 45 dB. From figure 4.8, the near-identical effect of using dilated switches and when allowing slot reuse at a node downstream to the destination node is observed. This is probably due to the fact that the downstream slot-release is almost the same architecture as a dilated switch, but only with a long piece of fiber between the switches.

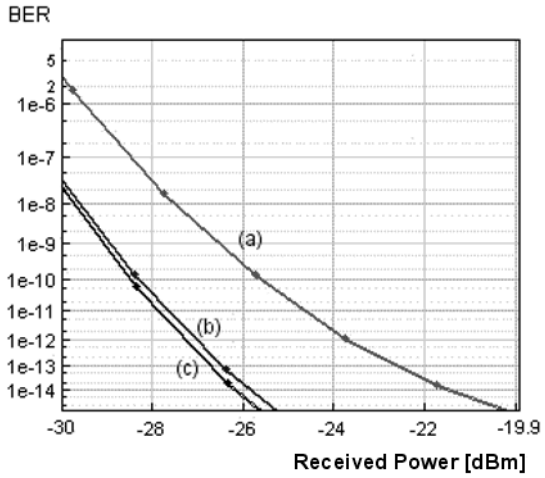

Figure 4.8: BER performance for a connection with 3 intermediate transparent nodes by (a) allowing slot-reuse at the destination node and using 2x2 switches; (b) allowing slot-reuse at a downstream node and using 2x2 switches; and, (c) using dilated switches.

4.3.3 Trade-off between the delayed slot release and the dilated switch approaches

The advantage of the dilated switch approach over the restricted spatial reuse approach in reducing inband crosstalk becomes apparent when we think in terms of network utilization and throughput. In the dilated switch approach the effect is localized to one node of the network. Whereas in the other case the slot has to travel a link on the ring unutilized; this should intuitively lead to reduced maximum network throughput. To estimate this drop in slot utilization and network throughput we perform a stochastic simulation in C++.

In one of the bidirectional rings slots rotate in clockwise direction and in the other they rotate in a counter-clockwise direction. Each node on the ring is able to access both the bidirectional rings. The arrival process at all nodes is the same all throughout the simulation and comprises of fixed size packets arriving according to a homogeneous Poisson Process with rate λ. The rate, λ, thus uniquely determines the load arriving at any node on the ring and thus the total load offered to the ring. An empty slot upon arriving at a node decides whether to pick up a packet depending upon the packet's destination node. The decision is based purely on the location of the destination node in relation to

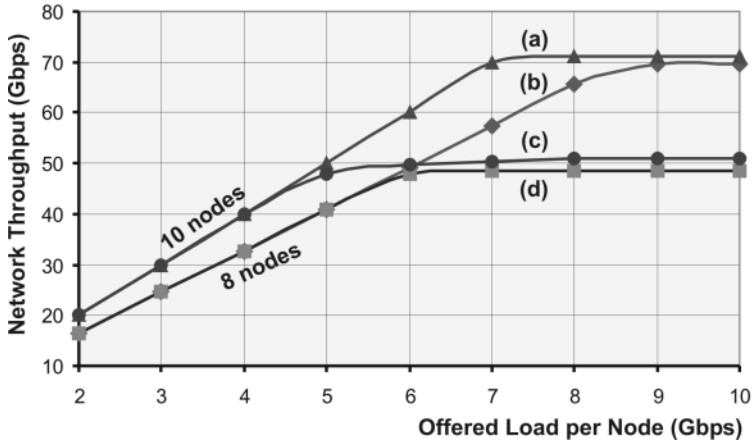

Figure 4.9: Network throughput: (a) and (b) dilated switches on a ring of 10 nodes and 8 nodes respectively; (c) and (d) restricting spatial reuse to one downstream node for a ring of 10 nodes and 8 nodes respectively

the source node and the direction of travel (clockwise or counter-clockwise) of the passing slot. Thus if a source node, A, has to send a packet to a destination node, B, and if node B is closest to node A in the clockwise direction, then a passing empty slot at A, only in the clockwise direction, is allowed to pick up this packet. Each node has fixed-size buffers implying loss of packets beyond a particular load. The results obtained are shown in figures 4.9 and 4.10. We see that both the network throughput and the slot utilization drop appreciably when spatial reuse is restricted to the downstream node. Intuitively this was expected, for slots were traversing an extra link on the rings unutilized. The following sections analyze and quantify in further detail the reason for this drop. However, the main drawback of the dilated switch approach as compared to the alternate approach of delayed slot release is that in the former the number of 2x2 $LiNbO_3$ switches per node doubles, including increased losses and thus a need for additional optical amplification (introducing extra noise).

4.4 Analysis of Results

The results of the previous section are analyzed here and are presented here in three categories. The first deals with the SNR degradation due to the EDFA-demultiplexer chain. The next analyses crosstalk accumulation in the ring.

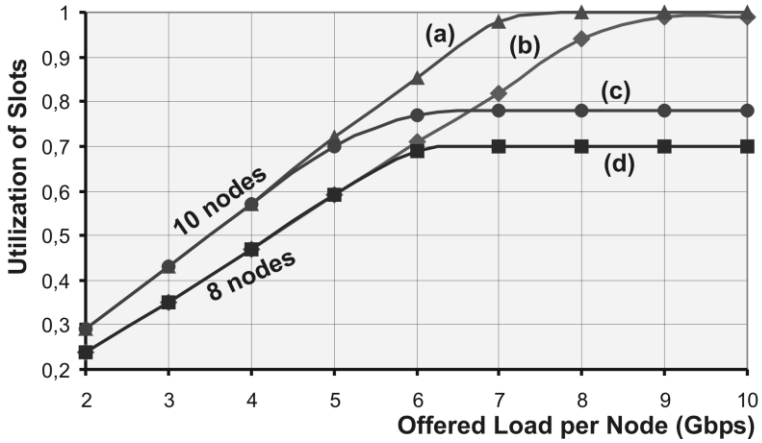

Figure 4.10: Network utilization: (a) and (b) dilated switches on a ring of 10 nodes and 8 nodes respectively; (c) and (d) restricting spatial reuse to one downstream node for a ring of 10 nodes and 8 nodes respectively.

Finally, the superior traffic performance achieved when using dilated switches instead of restricting slot reuse is analyzed.

4.4.1 Effect of EDFA-filter Cascade

In the previous section it was observed that the BER increases with an increase in the number of transparent nodes. This trend can be explained by analyzing the decreasing signal-to-noise ratio (SNR) with an increase in the number of transparent nodes. The decreasing SNR is primarily due to the EDFA-filter (demultiplexer) cascade and its effect can be analytically related to the plot of figure 4.7 as follows.

We know from [BOS'99] that the electrical SNR of a K-stage amplifier limited by signal-ASE beat noise is given by

$$SNR_{sig-ASE}^{K-stages} = \frac{P_{in}}{4h\nu B_e n_{ASE}(G-1)K} \tag{4.1}$$

where P_{in} is the average input signal power, $n_{ASE}(\geq 1)$ is the spontaneous noise emission factor, h is Planck's constant, ν is the optical frequency, G is gain of the EDFA, and B_e is the bandwidth of the electrical receiver. The optical SNR is obtained by multiplying equation (4.1) by $2 \times (B_e/B_o)$, where B_o is bandwidth

of the optical filter after the EDFA.

The noise figure for a system comprising of a chain of K optical amplifiers, with each amplifier providing a gain G to exactly compensate the loss L, is given by

$$F_{tot} = \frac{SNR^0}{SNR^K} = \frac{SNR^0}{SNR^1} \times \frac{SNR^1}{SNR^2} \times ... \times \frac{SNR^{K-1}}{SNR^K}. \tag{4.2}$$

The SNR ratios in equation (4.2) are the noise figures of each amplifier multiplied by $1/L$ since the amplifier noise figure is defined by the SNR's immediately prior and after the amplifier. In equation (4.2) each SNR_i is separated from the following amplifier by a span with loss, L. Thus the system noise figure, in logarithmin units, is be written as

$$F_{tot} = GF_1 + GF_2 + ... + GF_N = NGF \tag{4.3}$$

assuming all the amplifiers have an equal noise figure and $G = L$. Equation (4.3) implies that the SNR degradation (expressed in dB) in a cascaded amplifier transparent chain is linear with the number of amplifiers (assuming all amplifiers have the same noise figure). In figure 4.7, let us assume a power of -28 dBm. At this power plots (a), (b) and (c) have BERs of 6×10^{-4}, 3×10^{-8} and 10^{-13} respectively. If the noise is assumed to have Gaussian statistics (a relatively good assumption as the receiver modules in the simulation setup of section 4.3.1 were assumed to have Gaussian noise statistics), then the BER can be well approximated by:

$$BER = \frac{1}{\sqrt{2\pi}} \frac{\exp[\frac{-Q^2}{2}]}{Q} \tag{4.4}$$

where

$$Q^2 = \frac{SNR}{2}. \tag{4.5}$$

Figure 4.11 shows the plot of BER on a logarithmic scale versus Q. From equations (4.4) and (4.5) the SNR values for plots (a), (b) and (c) are 108.04, 58.75 and 21.26 respectively. From equation 4.2 the SNR degradation of the second stage (second transparent node) then equals 2.65 dB. Similarly, the SNR degradation of the third stage (third transparent node) then equals 4.4 dB, which is slightly less than the simulated noise figure of 5 dB of the EDFA. This discrepancy can be explained by the demultiplexer, which acts as a passband filter reducing ASE-ASE beat noise at the receiver.

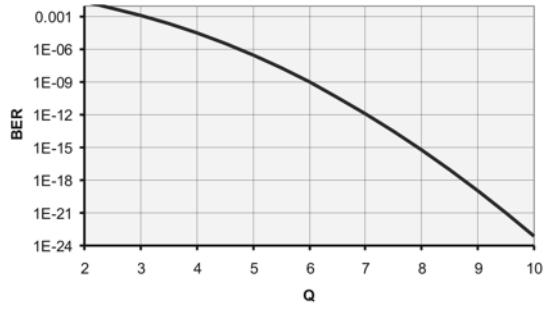

Figure 4.11: BER versus Q

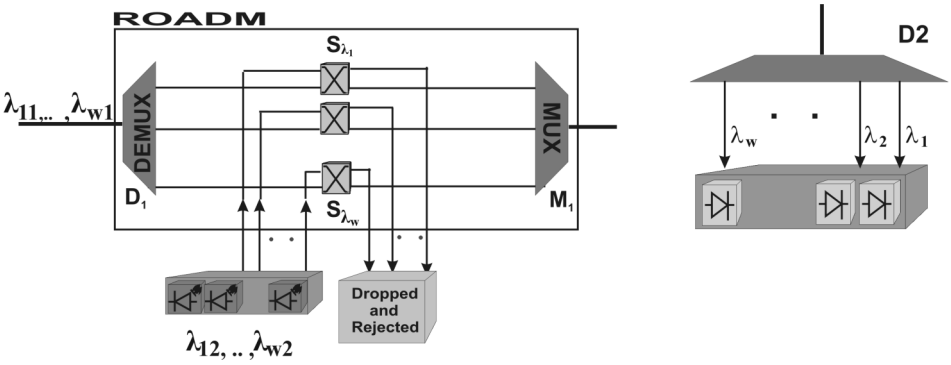

Figure 4.12: Model for Crosstalk Analysis

4.4.2 Effect of Crosstalk

Assume a connection from a source node A to a destination node B passing through a few intermediate nodes. Then at node A packets corresponding to the connection are added using a ROADM. At each of the intermediate nodes they pass through a ROADM. However at the destination node they do not pass through a ROADM. Here optical power is split and wavelength demultiplexed. Subsequently wavelength channels, including the one containing the packets, are received. It is also assumed that slots are ready for reuse at their destination nodes and normal 2x2 switches are used.

Assume the model shown in figure 4.12. Demultiplexer D_2 corresponds to the node that has to receive on channel λ_1. The ROADM in the figure corresponds to that of the previous upstream node. Let the number of WDM channels be denoted by W. As is the case with the network architecture of chapter 2, we

assume that the space switches route channels of the same wavelength. The following discussion is limited to the first and second order crosstalk terms. Third and further order crosstalk terms are neglected.

We now try establishing the total number of first order and second order contributions at the output of the demultiplexer, D_2. At the receiver corresponding to wavelength λ_1 we have the following situation:

- Crosstalk due to optical inband crosstalk terms arising from λ_1; and,
- Crosstalk due to optical outband crosstalk terms arising from $\lambda_2, .., \lambda_W$.

The optical inband crosstalk terms are attributed directly to the poor isolation of the fast 2x2 switches. We have two possibilities; one in which the transmitter corresponding to λ_{12} of the previous upstream node is OFF and the corresponding switch is in BAR state, and the other in which the same transmitter corresponding to λ_{12} is ON and the switch is in CROSS state. These states are related to bypassing of slots or to dropping/adding of data packets from/to slots respectively. The assumption of the transmitter being OFF is a reasonable assumption. This is because in the absence of data, modulation current is almost zero (assuming NRZ modulation) for a directly modulated DFB laser, leading to a sharp drop in (at least 25 dB) the output power of the transmitter.

When the transmitter corresponding to λ_{12} is ON, we have at the exit of the multiplexer, M_1 the main signal, λ_{12}, followed by the next optical inband crosstalk terms:

- **First order**: λ_{11} from the previous (first) upstream node, being suppressed once at the switch;
- **Second order and accumulating**: λ_{11} from the second upstream node, being suppressed twice by the switches at two nodes.

When the transmitter corresponding to λ_{12} is OFF, we have at the exit of the multiplexer, M_1 the main signal, λ_{11}, followed by the following optical inband crosstalk terms:

- **First order and accumulating**: λ_{11} from the node, which is upstream to the node at which the main signal originated. This is being suppressed once at the switch;
- **Second order and accumulating**: λ_{11} from the second upstream node, being suppressed twice by the switches at two nodes.

The optical outband crosstalk terms at the receiver corresponding to λ_1 can be obtained as follows. Demultiplexer D_2, in front of the receiver gives rise to first order optical inband crosstalk terms, $\lambda_2, .., \lambda_W$. The crossconnect from the previus upstream node gives rise to second order optical inband crosstalk terms, $\lambda_2, .., \lambda_W$.

Thus it is easy to conclude that including accumulating terms and neglecting third order terms a signal from its source to its destination is accompanied by one first order optical inband crosstalk term and W second order crosstalk terms. Out of these W second order crosstalk terms, one is optical inband and the remaining W-1 are optical outband crosstalk terms. This implies that for any connection, irrespective of the number of intermediate transparent nodes, two accumulating optical inband crosstalk terms accompany the main signal (ignoring third and higher order crosstalk terms).

4.4.3 Effect of Delayed Slot Release

From figures 4.9 and 4.10 we observe the decrease in network throughput and slot utilization when adopting the policy of delayed slot release. The plots can be quantitatively understood as follows (a similar analysis has been provided in section 2.7.2). In the event that we have a bidirectional ring comprising of 8 nodes each of 4 wavelengths at 2.5 Gbps, we have an installed capacity of $2\times4\times2.5 = 20$ Gbps. A destination node which is only one hop away from its source can be reached in one way. Since the destination node's relative position can have two possibilities, namely clockwise and counter-clockwise, we have

P(reaching a node one hop from its source) = 2/7;

P(reaching a node two hops from its source) = 2/7;

P(reaching a node three hops from its source) = 2/7; and,

P(reaching a node four hops from its source) = 1/7; this can be reached either clockwise or anti-clockwise.

$\Rightarrow$ Average distance travelled by a slot $= (2/7 \times 1) + (2/7 \times 2) + (2/7 \times 3) + (1/7 \times 4) = 16/7$ nodes.

$\Rightarrow$ Maximum Throughput the network can support $= 20 \times (\frac{8}{16/7}) = 70$ Gbps. This is observed in figure 4.9. That curve (a) in the figure is slightly beyond 70 Gbps is attributable to a round-off error of the number of slots that exist on the ring. The exact number of slots that can be accomodated on the ring comprises of a whole number and a fraction. This fraction has been rounded-off to 1.

In the situation that we restrict reuse of a slot to two downstream nodes

after the destination node we have the following:

Average distance travelled by a slot = $(2/7 \times 1) + (2/7 \times 2) + (2/7 \times 3) + (1/7 \times 4) + 1 = 23/7$ nodes.

$\Rightarrow$ Maximum Throughput the network can support = $20 \times (\frac{8}{23/7}) = 48.7$ Gbps, which can be seen in figure 4.9. This implies a drop in throughput of almost 47%. Accordingly the slot utilization should also drop by the same figure, which is observed in figure 4.10. Similarly the network throughput and utilization can be calculated for a ring with 10 nodes.

4.5 Conclusions

From the simulation results of section 4.3.2 it is observed that at a BER of 10^{-14} and a received power greater than -20 dBm a single bi-directional optical ring is able to support up to 8 optically transparent nodes. The BER performance of such a ring is predominantly affected by the SNR degradation due to the EDFA-filter (demultiplexer) cascade (section 5.1). The crosstalk traversing the ring is primarily inband and does not accumulate beyond one first-order crosstalk term for any connection with any number of intermediate transparent nodes. This inband crosstalk term can be reduced by either using dilated switches at the nodes or by restricting slot-reuse to the next downstream node after the slot's destination node (thereby restricting spatial reuse of a slot). The effect on the BER performance of either approach is similar even though the dilated switch approach results in additional optical amplification. However, the former approach scores over the latter when traffic performance criteria as network throughput and slot utilization are simulated. Experimentally we have also demonstrated and verified the slot-synchronization concept at a node.

In section 4.2.4 it has also been shown how the header processing functions have been simulated to obtain encouraging results. Their actual implementation is discussed in the next chapter. The processor time (delay) is mainly determined by the length of the headerpacket. The VHDL description can be too generic when speeds required are close to the limits of the hardware. Optimization with knowledge of the underlying hardware is then necessary.

CHAPTER 5

Laboratory Demonstrations

5.1 Introduction

In chapters 2 and 3 the concept of the slotted ring all-optical packet-switched metropolitan area network was introduced. In chapter 3 it was shown that the most important part of the node (and, thus of the network itself) is the header processor unit. The design and functions of the header processor unit were described in section 3.5. Figures 3.13 to 3.17 indicated the block diagram of the header processing functions and the underlying issues. In chapter 4 the simulation results of the header processing functions have been presented in figures 4.3 and 4.4. Following up on these preparations, in section 5.2 the realization of some of the header processing functions is described, and also the evaluation of those in laboratory experiments.

In section 5.3 we present the effect of cascading EDFAs interleaved with multiplexer/demultiplexers on system power penalties due to SNR degradation. Finally in section 6.1 we present our conclusions.

5.2 Demonstration of the Header Processing Functions

A portion of the node in figure 4.5 has been experimentally demonstrated to verify the ability of the HPU to control the slot-alignment and the add-drop switches. The demonstrator comprised of two major function blocks, the header processor itself and its surrounding components and the optical part comprising of the transmitters, the receivers and the optical switches. The setup is first discussed in section 5.2.1 and then the results are presented in section 5.2.2.

5.2.1 Setup

The experimental setup is shown in figure 5.1. The setup comprises of the HPU which receives slot headers from the data generator. The data generator also sends two types of packets, packet A and packet B, to the two transmitters labelled transmitter A and transmitter B respectively. Packets A from transmitter A correspond to slot headers from transmitter C arriving at the HPU. The information contained in these slot headers determines whether the 2x2 switch has to reconfigure to enable dropping a packet A and adding a packet B in its place or to allow packet A to pass through. The information also determines if packet B has to be transmitted and, if so, when it is to be transmitted. The outputs of the switch are then observed at the oscilloscope.

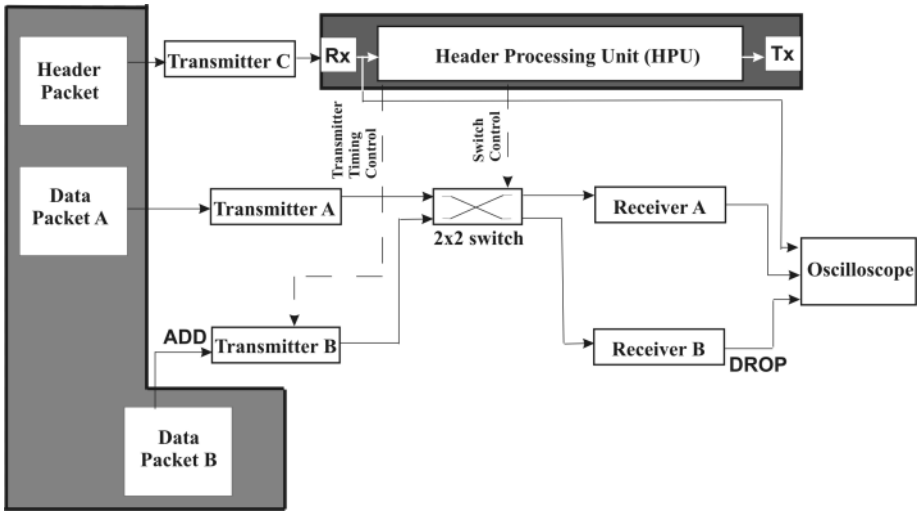

Figure 5.1: Demonstrator

The modulation speed was set at 155 Mbps. The HPU was realized using an Altera Field Programmable Gate Array (FPGA). The receiver module to receive the slot header and the transmitter module to send out the new slot header were implemented on the same printed circuit board along with the FPGA. The final PCB is shown in figure 5.2. The transmitter modules comprised of directly modulated DFB lasers. All the transmitters had an extinction ratio of roughly 8.2 dB and an average output power of 0 dBm. Transmitters A and B were at 1555.7 nm while transmitter C was at 1552.52 nm. PIN photodiodes were used for the receiver modules. A 2x2 $LiNbO_3$ switch was used for adding/dropping data signals. Length of a slot was 500 bytes ($\approx$ 25.8 μsec). The gap between slots was 2 bytes ($\approx$ 0.1 μsec). The header packets comprised of two 16-bit delimiters with 8 bits of information between them, thus having a total length of 40 bits. This structure of the header packet has no relation to the real MAC and has been adopted only to verify the physical layer concept of switching and transmitter-timing control. The FPGA, after analyzing these 8 bits, sends out 2 signals. One of the signals controls the switch. The other controls the precise time when transmitter B has to transmit.

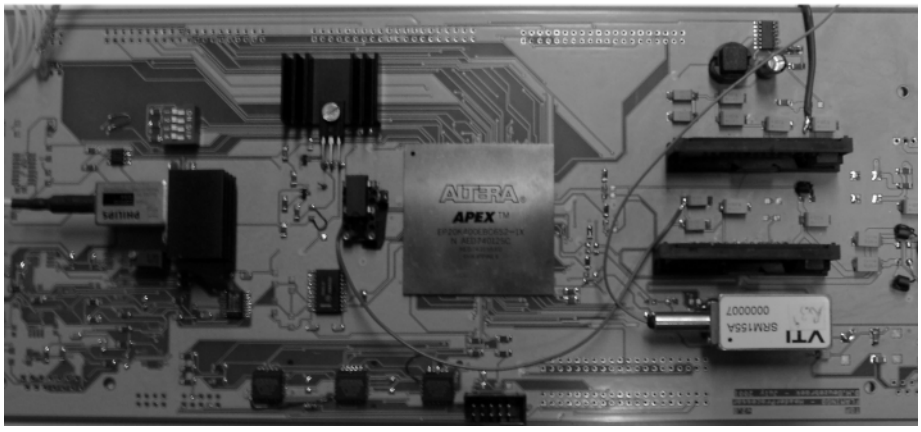

Figure 5.2: The HPU Printed Circuit Board

5.2.2 Results

Figure 5.3 shows the switching of slots from the transmitters A and B of figure 5.1. Slot A, coming from transmitter A, is the one that oscillates faster between ones and zeros, whereas the slower one corresponds to slot B, originating in

transmitter B. In figure 5.3, trace 4 corresponds to the output of receiver B and trace 2 to the output of receiver A. Trace 3 corresponds to the arrival of the header slot.

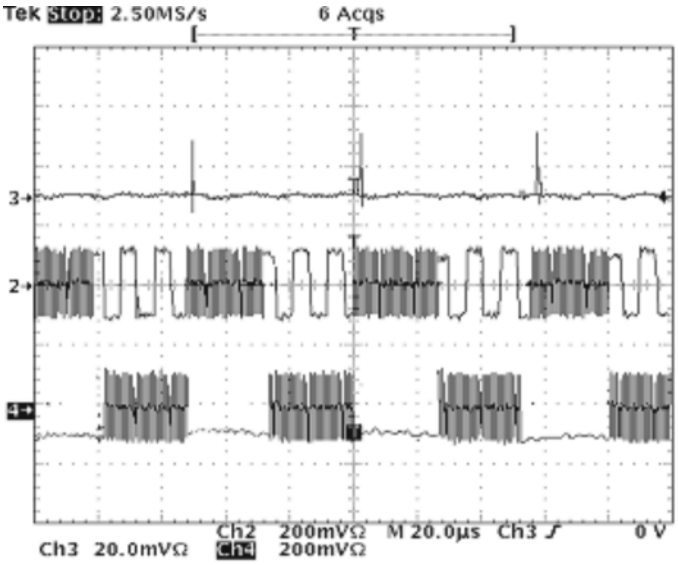

Figure 5.3: Laboratory Demonstration; each grid line on the horizontal axis is separated by 20 µs; on the vertical axis trace 3 corresponds to the header packet arriving at the PCB, trace 2 corresponds to output of receiver A and trace 4 corresponds to output of receiver B.

As mentioned in section 5.2.1 the header slot comprises of a packet of 40 bits. The delay between the instant that the first bit of the header packet arrives to the instant that the HPU sends out the switch control and the transmitter control signals is roughly 329 ns. This delay is induced by two stages. The main stage is getting the 40 bits into the FPGA. This takes 40 bit-times, which is roughly 258 ns at 155 Mbps. The second stage is the actual processing which takes 11 bit times (approx. 71 ns). This is because we used 11 registers between the incoming data signal and the outgoing data signal. After the switching signal was sent from the HPU to the switch the response time of the switch was less than 10 ns. However the response time of the transmitter timing control signal was quite high, about 0.5 μs. Analytically it was difficult to precisely pinpoint this value or put it in a tight range. However, we observed that by reducing the gap between the arrival of the first bit of the header slot and that of the first

bit of slot A (from transmitter A) to 16 bytes (820 ns), the BER of the received data rises substantially. Calculating backwards and subtracting the processing delay at the HPU we find that the response time of the transmitter unit was roughly 0.5 μs. The response time can be made a lot better by incorporating buffers on the same board as the transmitters themselves. However this is not the aim of the demonstration. Thus we see that the transmitter's timing can be set by a control signal from the HPU, implying that all the transmitters on all wavelengths can be made to transmit all with a fixed average delay.

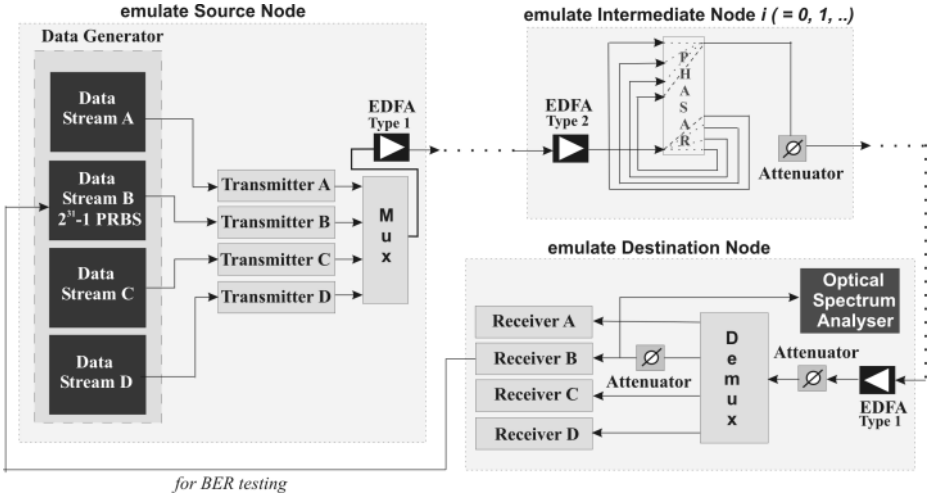

Figure 5.4: Setup to understand SNR degradation with increasing number of Intermediate Nodes

5.3 Cascading EDFAs with Multiplexer/ Demultiplexer

The aim of the experiment is to estimate the increase of power penalty when the number of intermediate nodes for a connection from its source node to its destination node is increased by one. The initial setup (shown in figure 5.4) comprised of 4 wavelength channels separated by 400 GHz. The source node, the intermediate nodes and the destination node are emulated as shown in the figure. The source and destination node make use of a thin-film multiplexer/demultiplexer whereas the intermediate nodes (forming a cascade) used Phasars. The EDFA compensates for power loss as shown in the figure. In a

second setup all Phasars were removed from the cascade and a series of EDFAs in cascade was tested for their BER performance. The number of EDFAs in the cascade in both the setups was varied between 1 and 6. The channels at the end of the cascade were demultiplexed and subsequently detected by receivers. One of the wavelength channels was then subjected to BER measurements.

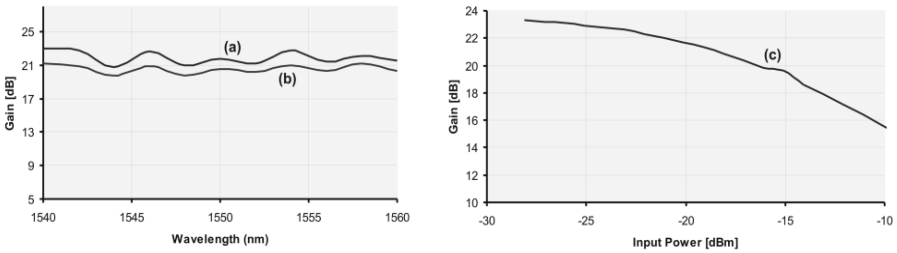

Figure 5.5: EDFA Type 1 Characteristics: (a) Gain versus wavelength profile at 50% of the maximum pump power and (b) at 25% of the pump power for an input power of -18 dBm; (c) Gain versus Input power for a single channel at 1552.52 nm and at 50% of the maximum pump power

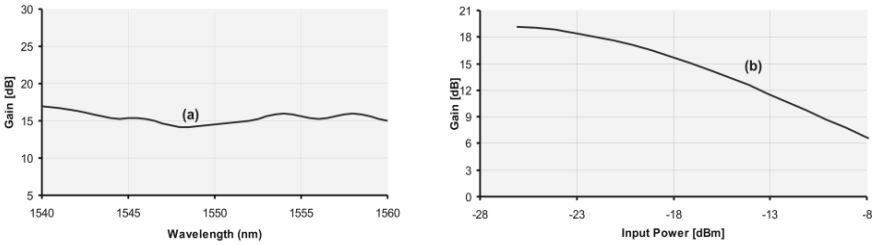

Figure 5.6: EDFA Type 2 Characteristics: (a) Gain versus wavelength profile for an input power of -18 dBm; (b) Gain versus Input power for a single channel at 1552.52 nm and at maximum pump power

Care was taken to ensure that the power of the optical signal entering the EDFAs in both the setups was held constant and that the EDFA was made to pump at the small signal gain region. This is to ensure a high gain and therefore a relatively more stable signal-to-noise ratio performance of the EDFA. The setups above were also repeated with a single channel only.

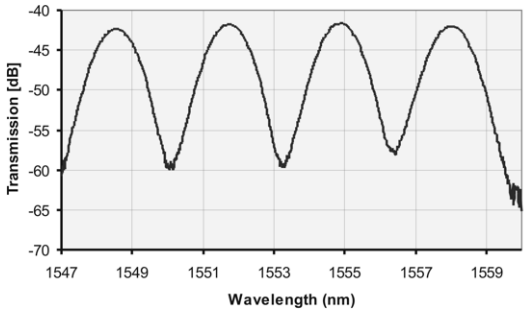

Figure 5.7: Phasar Characteristics

5.3.1 Setup

The setup comprised of the following key components.

- Transmitters: The transmitter modules comprised of directly modulated DFB lasers. All the transmitters had an extinction ratio of roughly 8.2 dB. Wavelength deviation of the transmitters was less than 100 pm in the total experiment. The transmitters had a spectral width of roughly 0.4 nm at -20 dB under modulation and an average output power of 0 dBm. Transmitter B (see figure 5.4) was modulated with a 2.5 Gbps $2^{31} - 1$ PRBS data stream. The remaining transmitters were modulated with 155 Mbps data patterns. The transmitters were all on the ITU grid and spaced by 400 GHz with Transmitter B at 1552.52 nm.

- Receivers: Receiver B of figure 5.4 comprised of an APD detector with a sensitivity of -31 dBm at a BER of 10^{-9}. This receiver was used for BER measurements. The other receivers comprised of PIN photodiodes.

- EDFAs Type 1: The EDFAs had a maximum noise figure of 7.5 dB. They were always operated in the small-signal gain region. The EDFA characteristics are shown in figure 5.5. The pump power of type 1 EDFAs could be varied.

- EDFAs Type 2: The EDFAs had a maximum noise figure of 7.5 – 8 dB. They were always operated in the small-signal gain region. The EDFA characteristics are shown in figure 5.6. The pump power of type 2 EDFAs could not be varied.

- Phasars: The Phasar characteristics are shown in figure 5.7. The characteristics were measured using a broadband source. They had a temperature shift of maximum 0.1 nm/°C and had a crosstalk of -30 dB. The Phasars were used in a foldback configuration. For more information on phasar configurations refer [Vee'99]. The foldback configuration introduces a substantial crosstalk penalty. Using a double phasar (each separate as a multiplexer or demultiplexer) reduces crosstalk but increases the chance of misalignment between the passbands.

- Multiplexer/Demultiplexer: The multiplexer and demultiplexer in the source and destination nodes respectively comprised of thin film filters and had an adjacent channel isolation of at least 35 dB.

5.3.2 Results

The results of the experiment are shown in figure 5.8. The figure shows the power penalty with an increasing number of EDFAs or EDFA/Phasar concatenations when comparing case (a) with case (b) and case (c) with case (d). It is important to realize that it is not correct to compare case (a) or case (b) with case (c) or case (d). This is because in the situation when there is only 1 EDFA, case (a) is the same as case (b) and case (c) is the same as case (d). All values of power penalty in the figure are obtained at a BER of 10^{-9} and is based on using 1 EDFA. Thus in the figure power penalty at 5 EDFAs, for instance, is equal to the difference in the required received power when using 5 EDFAs and when using 1 EDFA at a BER of 10^{-9}.

When comparing cases (a) and (b), it was expected from section 4.4.1 that the use of filters would reduce the ASE and thereby improve the SNR leading to a lower BER. Thus case (b) leads to a power penalty when compared with case (a). However the two curves crossover beyond a particular point. This can be explained by the fact that the Phasar passbands are temperature controlled and thus drift to a certain extent. This leads to passband narrowing of the main signal. Beyond a certain number of Phasars it affects the signal itself and increases the BER. Cases (c) and (d) depict a similar behaviour when using a single channel.

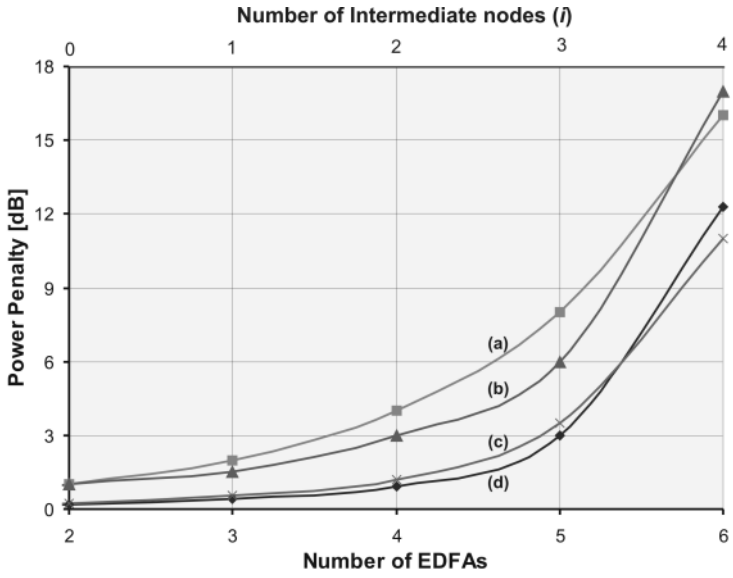

Figure 5.8: Power Penalty at BER $= 10^{-9}$*: (a) cascading EDFAs with 4 wavelength channels; (b) cascading Intermediate nodes with 4 channels; (c) cascading EDFAs with a single wavelength channel; (d) cascading Intermediate nodes with a single wavelength channel*

5.4 Conclusions

From the demonstrator it has been shown that it is possible to precisely control the transmitter-timing signal and with this control over transmitter timing it is possible to compensate for chromatic dispersion, which leads to slots losing their mutual synchronization. The processing of slot headers at a line speed of 155 Mbps have been tested. The HPU functions as described in section 3.5 and simulated in section 4.2. Switching of data packets using the control signal from the HPU has also been demonstrated.

The effect of cascading EDFAs and Phasars have also been experimentally demonstrated. The Phasars limit the SNR degradation due to the EDFA cascade to a certain extent, but beyond that the narrowing of the passband of the complete system plays an significant role in degrading the system itself. Thus significant benefits can be obtained from passband flattened (de)multiplexers and their stable characteristics.

CHAPTER 6

Conclusions and Directions for Further Research

The scope of research in all-optical networks, enabling packet-switching and optical multicasting, is in itself so broad and so diverse that it deserves far more attention than what has been provided in this work. Section 6.1 presents the conclusions from the various chapters and then draws a global overview of what has been achieved and can be concluded from this work as a whole.

Strictly speaking the list of directions for further research could be never-ending. However a small list has been provided in section 6.2 on very specific areas of research, which have been dealt with in this thesis and which require far more attention.

6.1 Conclusions

Slotted-ring Network Architecture for MAN: The use of a ring-based interconnected network in the MAN space provides numerous advantages, including: (1) there is only one path (assuming a connection takes the shortest of the clockwise and the counter-clockwise paths) between any two points on the network, so that the ordering of packets is always maintained, (2) information

can be sent from one point in the network to one or more other points, providing a natural multicast mechanism, and (3) a simple routing scheme can be used, allowing for high-speed operation of the rings and (4) build on existing ring-based infrastructure in the MANs. For any multicast connection there exist at most two branches, separated at the source. One of them is clockwise and the other counter-clockwise. Using counter-rotating rings also facilititates protection of the individual rings.

The concept of transporting packets using slots enables IP packets to be transported over WDM with relative ease. It preserves the data packets in the optical domain enabling bit-rate and protocol transparencies. It is also possible to support all-optical multicasting.

Node Architecture of the Slotted-ring: The node architecture was gradually built-up by first identifying and analyzing the system issues enforced by the network architecture and others that go hand-in-hand with optical fiber networks in general. Key issues include slot synchronization, optical multicasting, crosstalk, power budget and timing-control. Types of node architectures prevalent in today's WDM network were discussed in section 3.3. Consequently a block schematic diagram of the node was proposed in section 3.4. Using this as the reference, technologies for each of the blocks were analyzed and preferences were presented. Key features of the proposed node include supporting all-optical packet switching and optical multicasting and being optically transparent to data packets.

Proposals were made to tackle each of the system design issues. Finally, a power budget calculation was made in section 3.11 and the complete node architecture depicted in figure 3.21. The power budget calculations indicate that the received power at the receivers is around -7 dBm and thus there is enough system margin for power penalty from crosstalk and other signal degradations.

Performance of the Network and Node Architectures: From the simulation results of section 4.3.2 it is observed that a single bidirectional optical ring with 8 wavelength channels is able to support up to 8 optically transparent nodes spaced 20 kilometers apart. The BER performance of such a ring is predominantly affected by the SNR degradation due to the EDFA-filter (demultiplexer/multiplexer) cascade (section 5.1). The crosstalk traversing the ring is primarily inband and does not accumulate beyond one first-order crosstalk term for any connection with any number of intermediate transparent nodes. This inband crosstalk term can be reduced by either using dilated switches at the nodes or by restricting slot-reuse to the next downstream node after the slot's

destination node (thereby restricting spatial reuse of a slot). The effect on the BER performance of either approach is similar. However, the former approach scores over the latter when traffic performance criteria as network throughput and slot utilization are simulated.

In section 4.2.4 the header processing functions have also been simulated. The simulation provides an insight into timing control issues of the HPU. There also we obtained encouraging results such as the ability to read the incoming slot headers, control the switches, the receivers and the transmitters and generate new slot headers in a timely-manner that preserves the mutual synchronization of slots and enables adding/dropping of data packets.

Experimental Results: From the demonstrator it has been shown that it is possible to precisely control the transmitter-timing signal and thus compensate for chromatic dispersion, which would lead to slots losing their mutual synchronization. The processing of slot headers at a line speed of 155 Mbps has been tested. The HPU functions as described in section 3.5 were simulated in section 4.2. Switching of data packets using the control signal from the HPU has also been demonstrated.

The effect of cascading EDFAs and Phasars has also been experimentally demonstrated. The Phasars limit the SNR degradation due to the EDFA cascade to a certain extent, but beyond that the narrowing of the passband of the complete system plays a significant role in degrading the signal itself. The degradation is due to the intensity loss of the chirped laser from the narrowed passband of the Phasar cascade. Thus significant benefits can be obtained from passband flattened (de)multiplexers and their stable characteristics.

General Conclusions: In this thesis a novel concept for building a packet-switched MAN with support for multicasting in the optical domain has been presented. The MAN comprises of interconnected all-optical rings. Slots transport data packets within each ring all-optically. This enables optical packet-switching at intermediate nodes on a ring. The nodes are capable of transmitting and receiving at all wavelengths. This increases the throughput of each ring due to spatial reuse of slots. In crossing over from one ring to another data packets undergo opto-electronic conversion. This is primarily needed due to the non-availability of optical buffers. Problems such as slot-synchronization (chromatic dispersion), crosstalk accumulation and SNR degradation have been simulated, analyzed and/or experimentally demonstrated. In addition, the feasibility of the HPU and some of the processing functions involved in adding and/or dropping data packet to and/or from a ring have also been demonstrated. Based on

this it has been concluded that it is possible to build a bidirectional optical ring with upto 8 nodes. The main factor limiting the scalability of the all-optical ring is the EDFA-Phasar cascade. The EDFA cascade on one hand degrades the SNR. On the other hand, although the Phasar cascade reduces ASE from the EDFAs, their passband narrowing affects the signal substantially. The crosstalk traversing and accumulating in the ring is optical inband crosstalk, arising from the poor isolation of the fast $LiNbO_3$ switches. However the generation of this type of crosstalk can be reduced to a large extent by using dilated switches or by postponing the spatial reuse of a slot to a downstream node with relation to the node where it is released. Chromatic dispersion, leading to slot misalignment, can be compensated by precisely controlling the signal which commands the data generator to start sending data.

6.2 Directions for Further Research

Passband-flattened Phasars: It has been shown in section 5.3.2 that the performance of the system was limited by the passband narrowing of the Phasar cascade. This can be improved by the use of Phasars with passband-flattened characteristics and improving the temperature stabilization process. This will ensure that the Phasars do not drift too much with temperature and that the laser wavelengths remain within the flat passbands.

Increasing the line-speed of the header channel: The HPU functions have been tested to work correctly at a line speed of 155 Mbps. It could have been easily upgraded to 622 Mbps because the Altera FPGA can handle those speeds. The linespeed of the header channel and that of the data channels may differ in an actual network setup. However a slower line speed on the header channel implies a larger fiber delay line for the data channels. This is because in chapter 4 it has been shown that the major part of the total header processing time is consumed in taking in the bits and sending them out one by one. Therefore it would be interesting to look into alternative techniques where line-speeds in excess of 2.5 Gbps can be handled. Also, the header channel being newly generated at each node can tolerate much more signal degradation than the data channels. Thus other modulation techniques can be thought of to put more bits within one clock cycle. This will directly reduce the header processing time and thus the length of the fiber delay lines. In section 5.2.2 it was found that the header processing delay was 329 ns (assuming the header structure of

section 5.2.1), equivalent to roughly 65.8 m.

Nodes interconnecting rings: In section 2.7.4 we have used a crude way of transporting slots between rings, namely store and forward. This involves conversion into the electronic domain and back to the optical domain. This can be analyzed in more detail and more efficient techniques can be thought of. For instance, it would be interesting to use optical buffers.

SNR Analysis: Models could be used to analyze the SNR degradation of the signal when using non-passband-flattened Phasars along with their individual temperature drift, causing misalignment. This could quantify the importance of using passband-flattened Phasars and their temperature stabilization.

List of Acronyms

AHDL	Altera Hardware Description Language
AOTF	Acousto Optic Tunable Filter
APD	Avalanche Photo Diode
APS	Automatic Protection Switching
ASE	Amplified Spontaneous Emission
ATM	Asynchronous Transfer Mode
AWG	Arrayed Waveguide Gratings
BER	Bit Error Rate
CD	Collision Detection
CDM	Code Division Multiplexing
CSMA	Carrier Sense Multiple Access
CVPD	Chemical Vapour Phase Deposition
CWDM	Coarse Wavelength Division Multiplexing
DCF	Dispersion Compensating Fiber
DFB	Distributed Feed Back
DG	Diffraction Grating
DSF	Dispersion Shifted Fiber
DTFF	Dielectric Thin Film Filter
DWDM	Dense Wavelength Division Multiplexing
ECT	Embedded Clock Transport
EDFA	Erbium Doped Fiber Amplifier
EOTF	Electro Optic Tunable Filter
FBG	Fiber Bragg Grating
FBTF	Fiber Brillouin Tunable Filter
F-P	Fabry-Perot

FDDI	Fiber Distributed Data Interface
FET	Field Effect Transistor
FFP	Fiber Fabry Perot
FLAMINGO	Flexible Multiwavelength Optical Local Access Network Supporting Multimedia Broadband Services
FPF	Fabry-Perot Tunable Filter
FPGA	Field Programmable Gate Array
FTP	File Transfer Protocol
GbE	Gigabit Ethernet
GMPLS	Generalized Multi-Protocol Label Switching
HPU	Header Processor Unit
HTTP	Hyper Text Transfer Protocol
IEEE	Institute of Electrical and Electronics Engineers
IETF	Internet Engineering Task Force
IP	Internet Protocol
ISI	Inter Symbol Interference
ITU-T	International Telecommunication Union -Telecommunication
LAN	Local Area Network
LER	Label Edge Router
$LiNbO_3$	Lithium Niobate
LSP	Label Switched Path
LSR	Label Switched Router
LVDS	Low Voltage Differential Signal
MAC	Medium Access Control
MAN	Metropolitan Area Network
MC	Multicast Capable
MEMS	Micro Electro Mechanical System
MON	Metropolitan Optical Network
MPLS	Multi-Protocol Label Switching
MZDCS	Mach-Zehnder Directional Coupler Switch
MZF	Mach-Zehnder Tunable Filter
NDF	Normal Dispersion Fiber
OADM	Optical Add Drop Multiplexer
OAM	Operations, Administration and Maintenance
OBS	Optical Burst Switching
OLS	Optical Label Switching
OLSR	Optical Label Switched Router
OPS	Optical Packet Switching
OXC	Optical Cross Connect
PCB	Printed Circuit Board
PDH	Plesiochronous Digital Hierarchy
PECL	Positive Emitter Coupled Logic
PLL	Phase Locked Loop
QoS	Quality of Service
RAM	Random Access Memory
RFC	Request For Comment

ROADM	Reconfigurable Optical Add Drop Multiplexer
RPR	Resilient Packet Rings
SBTF	Semiconductor-Based Tunable Filter
SCM	Sub-Carrier Multiplexing
SDH	Synchronous Digital Hierarchy
SiO_2	Silicon Dioxide
SLA	Service Level Agreements
SMF	Single Mode Fiber
SMTP	Simple Mail Transfer Protocol
SNR	Signal to Noise Ratio
SOA	Semiconductor Optical Amplifier
SONET	Synchronous Optical Network
SPM	Self Phase Modulation
SRP	Spatial Reuse Protocol
SWIS	Selective Wrap Independent Steer
TCP	Transmission Control Protocol
TDM	Time Division Multiplexing
TiO_2	Titanium Dioxide
TL	Tunable Laser
UDP	User Datagram Protocol
UTP	Unshielded Twisted Pair
VHDL	VHSIC (Very High Speed Integrated Circuit) Hardware Description Language
VPI	Virtual Photonics Incorporated
WAN	Wide Area Network
WDM	Wavelength Division Multiplexing

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APPENDIX A

VHDL code

```
-- file dataproc.vhd
--
-- Authors: Douwe Geuzebroek, Diptish Dey, Kees van Bochove, March 2001
--
-- description: data processing function for FLAMINGO Header
--                                                    processor
--
--              in: 8 bit data, 3 bit address, 3 bitmy_address,
--
--              SEND, flag_valid, reset and clock
--
--              out:ctrlsignals, 8 bit new data andvalid_out
--
--              all ports are of the std_logic type
--
--*********************************************************************

LIBRARY ieee; USE ieee.std_logic_1164.all;

--*********************************************************************

ENTITY dataproc IS
```

```
         PORT (data_in : IN  std_logic_vector(7 downto 0);
                          address_in, my_address_in: IN std_logic_vector(2 downto 0);
                      flag1_valid, SEND, reset, clk : IN std_logic;
                      data_out : OUT std_logic_vector(7 downto 0);
                      tristate_out, transm_timing, receiver_valid_out, valid_out :
                      OUT std_logic);
END dataproc;

--*********************************************************************

ARCHITECTURE behave OF dataproc IS
signal minislot1, minislot2, new_minislot1, new_minislot2 : std_logic_vector(3 downto 0);
signal new_address_in : std_logic_vector(2 downto 0);
signal tsend, tristate_out_i, transm_timing_i, receiver_valid_out_i,
valid_out_i, address_valid1, address_valid2 : std_logic;

BEGIN
-- assign incoming signals to local signals
                  minislot1 <= data_in(7 downto 4);
                  minislot2 <= data_in(3 downto 0);
                  tsend <= SEND;
                  new_address_in <= address_in;


        PROCESS(clk, reset, data_in, flag1_valid, SEND, address_in, minislot1, minislot2,
         tsend, new_address_in)
        BEGIN
-- check if the address in the header data is the same as my
address
                if my_address_in = minislot1(3 downto 1) then
                    address_valid1 <= '1';
                else address_valid1 <= '0';
                end if;
                if my_address_in = minislot2(3 downto 1) then
                    address_valid2 <= '1';
                else address_valid2 <= '0';
                end if;

-- when flag1_valid is 1 the data is valid and can be processed
                if flag1_valid = '1'  then

                -- set valid_out signal to 1
                    valid_out_i <= '1';
                    -- check minislot1
```

```
    -- if my address and full
    if address_valid1 = '1' then
        tristate_out_i <= '1';
        transm_timing_i <= tsend;

        -- new data generating
        if tsend = '1' then
            new_minislot1(3 downto 1) <= new_address_in;
            new_minislot1(0) <= '1';
        else
            new_minislot1 <= "0000";
        end if;
    else
-- if not my address and empty
        if minislot1(0) = '0' then
            tristate_out_i <= tsend;
            transm_timing_i <= tsend;

            -- new data generating
            if tsend = '1' then
                new_minislot1(3 downto 1) <= new_address_in;
                new_minislot1(0) <= '1';
            else
                new_minislot1 <= minislot1;
            end if;
-- if not my address and full
        else
            tristate_out_i <= '0';
            transm_timing_i <= '0';

            --new data generating
            new_minislot1 <= minislot1;
        end if;
    end if;

    -- check minislot2
    -- if my address
    if address_valid2 = '1' then
        receiver_valid_out_i <= '1';
        new_minislot2 <= "0000";
    -- if not my address
    else
        receiver_valid_out_i <= '0';
        new_minislot2 <= minislot2;
```

```
                end if;
        -- avoid latching of signals by stating them explicitely
                Else transm_timing_i <='0';
                    valid_out_i <= '0';
                    new_minislot1 <= "0000";
                    new_minislot2 <= "0000";
                    receiver_valid_out_i <= '0';
                    tristate_out_i <= '0';
                end if;
        -- register the internal signals to the output signals
                if reset = '1' then
                    data_out <="00000000";
                    valid_out <= '0';
                    tristate_out <= '0';
                    transm_timing <= '0';
                    receiver_valid_out <= '0';


                elsif (clk'event and clk = '1') then
                    data_out <= new_minislot1 & new_minislot2;
                    tristate_out <= tristate_out_i;
                    transm_timing <= transm_timing_i;
                    receiver_valid_out <= receiver_valid_out_i;
                    valid_out <= valid_out_i;
                end if;

        END PROCESS;

END behave;

--*********************************************************************

--              file cntr.vhd
--              Authors: Douwe Geuzebroek, Diptish Dey, Kees van Bochove, March 2001
--              description: one-time down counter for FLAMINGO Header Processor
--              counter for the serializer block
--              counts 40 clockpulses
--              in: Clock, valid and reset
--              out: valid_out
--
--              all ports are of the std_logic type
--
--*********************************************************************
```

```
LIBRARY ieee; USE ieee.std_logic_1164.all;

--*********************************************************************

ENTITY cntr IS

        PORT (clk, valid, reset: IN  std_logic;
              valid_out :     OUT std_logic);

        SIGNAL temp: integer range 0 to 39;

END cntr;

--*********************************************************************

ARCHITECTURE behave OF cntr IS BEGIN
        PROCESS(reset, clk)
        BEGIN
                IF RESET = '1' THEN

                temp <= 0;

                Elsif (clk'event AND clk = '1') then
-- when valid signal becomes high, load counter with 39
                        if valid = '1' then
                                            temp <= 39;
                                            valid_out <= '1';
-- after valid signal is down again count 39 clock pulses
                        else
                        if temp /= 0 then
                        -- during downcounting valid out =1
                            valid_out <= '1';
                            temp <= temp -1;
                        -- after downcounting valid_out = 0
                        else
                            temp <= 0;
                        valid_out <= '0';
                        end if;


                                end if;
                end if;
        END PROCESS;
END behave;
```

```
--**********************************************************************

-- file toggl.vhd
-- Authors Douwe Geuzebroek, Diptish Dey, Kees van Bochove, March 2001
--              description: toggles between 0 and 1 to generate clock pulses
--              used for serializer block in FLAMINGO Header Processor
--              in: clock, reset
--              out: toggle_out
--
--              all ports are of the std_logic type
--
--**********************************************************************

LIBRARY ieee; USE ieee.std_logic_1164.all;

--**********************************************************************

ENTITY toggl IS

        PORT (clk, reset: IN  std_logic;
              togglout :     OUT std_logic);
        SIGNAL toggltemp: std_logic;
END toggl;

--**********************************************************************

ARCHITECTURE behave OF toggl IS BEGIN
        PROCESS(reset, clk)
        BEGIN
-- reset values
                IF RESET = '1' THEN
                toggltemp <= '0';
                togglout <= '0';
-- toggle between 0 and 1
                Elsif (clk'event AND clk = '1') then
                         toggltemp <= not toggltemp;
                        togglout <= toggltemp;
                end if;
        END PROCESS;
END behave;

--**********************************************************************
```

APPENDIX B

Test Bench

```
-- file dataproc_test.vhd \\
-- description: test bench fordataproc.vhd \\
--              8 bit in, ctrl signals and new data out \\
--              timing model included
--              all ports are of the std_logic type \\
--
--************************************************************************

LIBRARY ieee; USE ieee.std_logic_1164.all;

--************************************************************************

ENTITY dataproc_test IS END;

--************************************************************************

ARCHITECTURE testbench OF dataproc_test IS
    type sample is record
        datin : std_logic_vector(7 downto 0);
        add_in : std_logic_vector(2 downto 0);
        my_add_in : std_logic_vector(2 downto 0);
        fl_vld : std_logic;
```

```
        send : std_logic;
        reset : std_logic;
        datout : std_logic_vector(7 downto 0);
        triout : std_logic;
        trmtim : std_logic;
        rec_val : std_logic;
        val_out : std_logic;
    end record;
type sample_array is array(natural range <>) of sample; constant
test_data : sample_array :=
    (
        ("00000000","100","010",'0','0','1', "00000000",'0','0','0','0'), --reset vector
        ("00000000","100","010",'0','0','0', "00000000",'0','0','0','0'),
        ("00000000","100","010",'0','0','0', "00000000",'0','0','0','0'),
        ("01011001","100","010",'1','1','0', "10011001",'1','1','0','1'),
        ("01011101","100","010",'1','0','0', "00001101",'1','0','0','1'),
        ("01010101","100","010",'1','0','0', "00000000",'1','0','1','1'),
        ("01010101","100","010",'1','0','0', "00000000",'1','0','1','1'),
        ("01010101","001","010",'1','1','0', "00110000",'1','1','1','1'),
        ("01010101","001","010",'0','1','0', "00000000",'0','0','0','0')

    );

component dataproc
    port(data_in : IN std_logic_vector(7 downto 0);
        address_in, my_address_in : IN std_logic_vector(2 downto 0);
        flag1_valid, send, reset, clk : IN std_logic;
        data_out : OUT std_logic_vector(7 downto 0);
        tristate_out, transm_timing, receiver_valid_out, valid_out : OUT std_logic);
end component; for all : dataproc use entity work.dataproc;

signal      datin : std_logic_vector(7 downto 0); signal
add_in : std_logic_vector(2 downto 0); signal      my_add_in :
std_logic_vector(2 downto 0); signal      fl_vld : std_logic;
signal      send : std_logic; signal      reset : std_logic;
signal      clk : std_logic; signal      datout :
std_logic_vector(7 downto 0); signal      triout, trmtim, rec_val,
val_out : std_logic; begin
    process
    begin
        for i in  test_data'range loop
        datin <= test_data(i).datin;
        add_in <= test_data(i).add_in;
        my_add_in <= test_data(i).my_add_in;
```

```
        fl_vld <= test_data(i).fl_vld;
        send <= test_data(i).send;
        reset <= test_data(i).reset;
        clk <= '0';
        wait for 3 ns;
        clk <= '1';
        wait for 3 ns;
        assert datout = test_data(i).datout
            report "data_out is wrong"
            severity error;
        assert triout = test_data(i).triout
            report "tristate_out is wrong"
            severity error;
        assert trmtim = test_data(i).trmtim
            report "transm_timing is wrong"
            severity error;
        assert rec_val = test_data(i).rec_val
            report "receiver_valid_out is wrong"
            severity error;
        assert val_out = test_data(i).val_out
            report "valid_out is wrong"
            severity error;
        end loop;
        wait;
    end process;
    CUT: dataproc port map (datin, add_in, my_add_in, fl_vld, send, reset, clk,
                datout, triout, trmtim, rec_val, val_out);
END;
```

APPENDIX C

Programmable Hardware

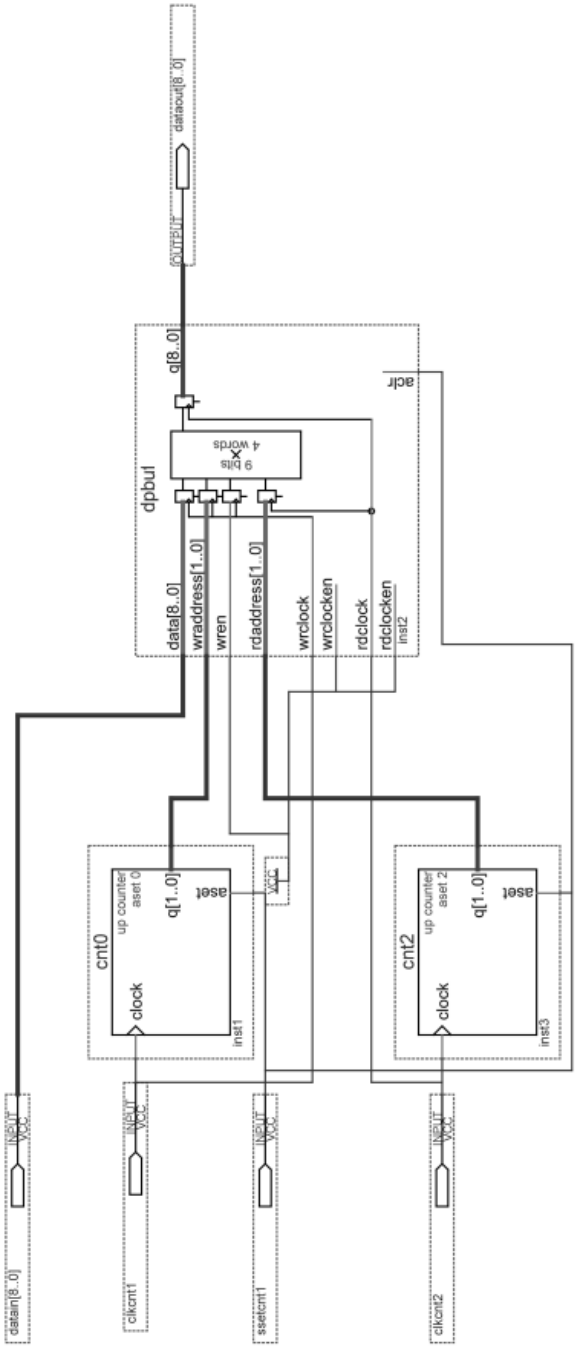

Figure C.1: DC Buffer

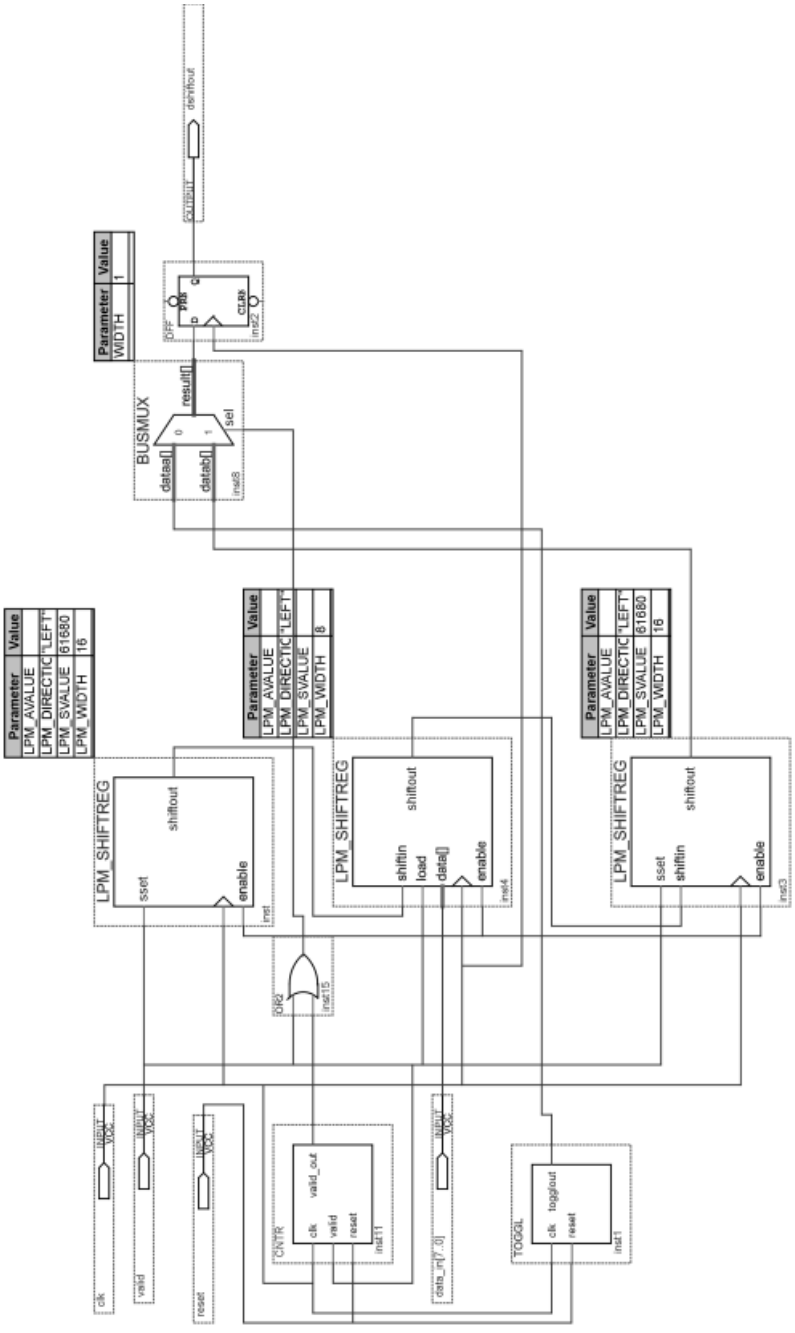

Figure C.2: Serializer

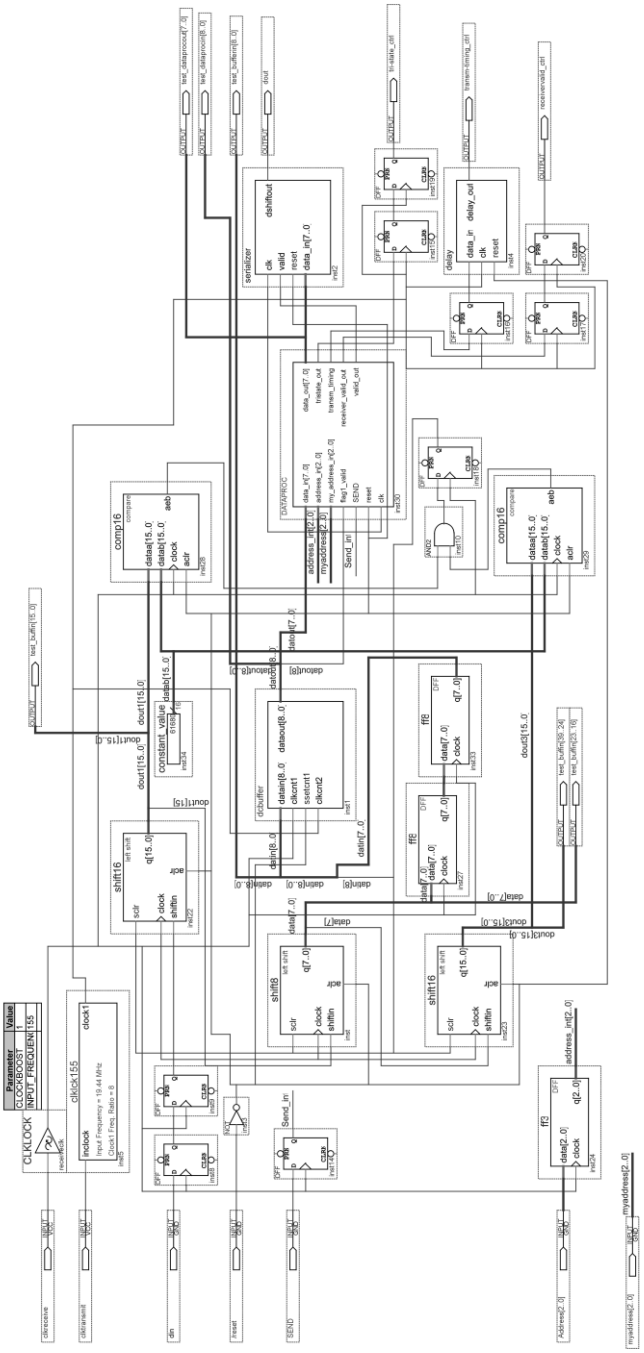

Figure C.3: Header Processor